Low Power Integrator and Comparator Design For Dual Slope ADC

Dissertation submitted to
Visvesvaraya National Institute of Technology, Nagpur
in partial fulfillment of the requirements for the award of the degree

Master of Technology
in
VLSI DESIGN

by

VEGI DORA APPALANAIDU (MT23MVD009)

Under the guidance of

Dr. Vasu Pulijala

Center for VLSI and Nanotechnology
Visvesvaraya National Institute of
Technology Nagpur 440 010 (India)

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I VEGI DORA APPALANAIDU, hereby declare that this dissertation titled, "**Low Power Integrator and Comparator Design For Dual Slope ADC**" is carried out by me in the Department of **Center for VLSI and Nanotechnology** of Visvesvaraya National Institute of Technology, Nagpur. The work is original and has not been submitted earlier whole or in part for the award of any degree/diploma at this or any other Institution / University.

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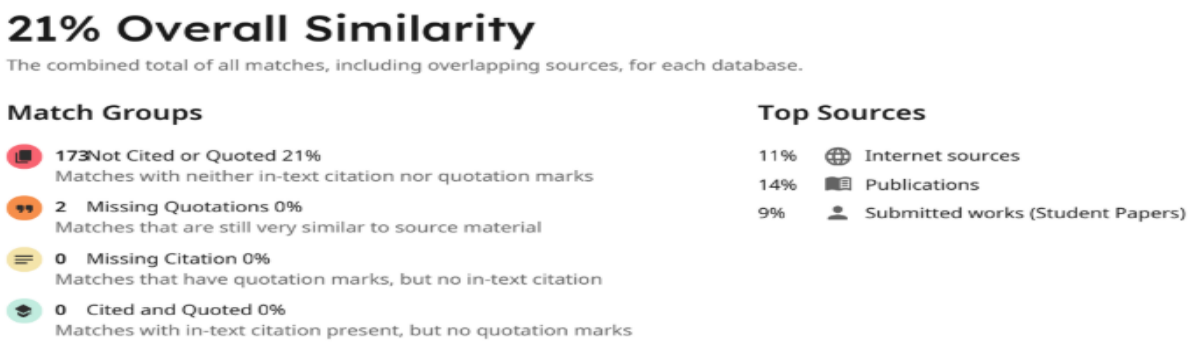
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ABSTRACT

In the rapidly advancing world of semiconductor technology, low-power and high-performance analog circuits are essential for various applications, including CMOS image sensors and analog-to-digital converters (ADCs). This thesis presents the design, analysis, and implementation of low-power analog circuits, with a primary focus on CMOS image sensors and dual-slope analog-to-digital converters (ADCs). Conducted as part of an internship, the project emphasized practical experience in analog circuit design and verification using Cadence Virtuoso. The core objective was to develop efficient analog building blocks for Readout Integrated Circuits (ROIC) in CMOS image sensors, including operational amplifiers, buffers, current mirrors, and ADCs.

The work began with the design and optimization of a dual-slope ADC, a robust architecture known for its high-resolution and noise-reduction capabilities. The design was enhanced with a bulk-driven two-stage operational transconductance amplifier (OTA), which provided improved performance at ultra-low power levels. A low-power comparator and integrator were also developed, optimized for precise signal conversion with minimal power consumption. For the CMOS image sensor, emphasis was placed on the readout circuit, where techniques such as correlated double sampling (CDS) and guard-ring protection were employed to enhance signal integrity.

Comprehensive simulations, including DC, AC, and transient analyses, were performed to validate the performance of these circuits across various operating conditions. Process, voltage, and temperature (PVT) variations were also considered to ensure design robustness. The results demonstrate the successful implementation of low-power, high-performance analog circuits suitable for high-precision applications, such as medical imaging, automotive systems, and portable devices.

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List of Abbreviations

ROIC	Read out Integrated Circuitry
CMOS	Complementary Metal Oxide Semiconductor
PVT	Process voltage temperature
ADC	Analog to digital
□□□	Overdrive Voltage
□□□	Threshold Voltage
ICMR	Input Common Mode Range
OCMR	Output Common Mode Range
OTA	Operational transconductance Amplifier
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
PPS	Passive Pixel Sensor
APS	Active Pixel Sensor
PD	Photo Diode
BD	Bulk Driven
DRC	Design rules check
LVS	Layout verses Schematic
VTC	Voltage Transfer characteristics

Chapter 1

Introduction

This internship focused on acquiring practical experience in analog circuit design and verification, particularly within the domain of CMOS image sensors. The primary emphasis was on the Readout Integrated Circuit (ROIC), a crucial component responsible for processing signals from the pixel array in image sensors.

CMOS image sensors are integral to various applications, including digital cameras, smartphones, medical imaging devices, and automotive systems. These sensors rely heavily on the performance of analog circuits to capture, amplify, and convert light signals into digital data.

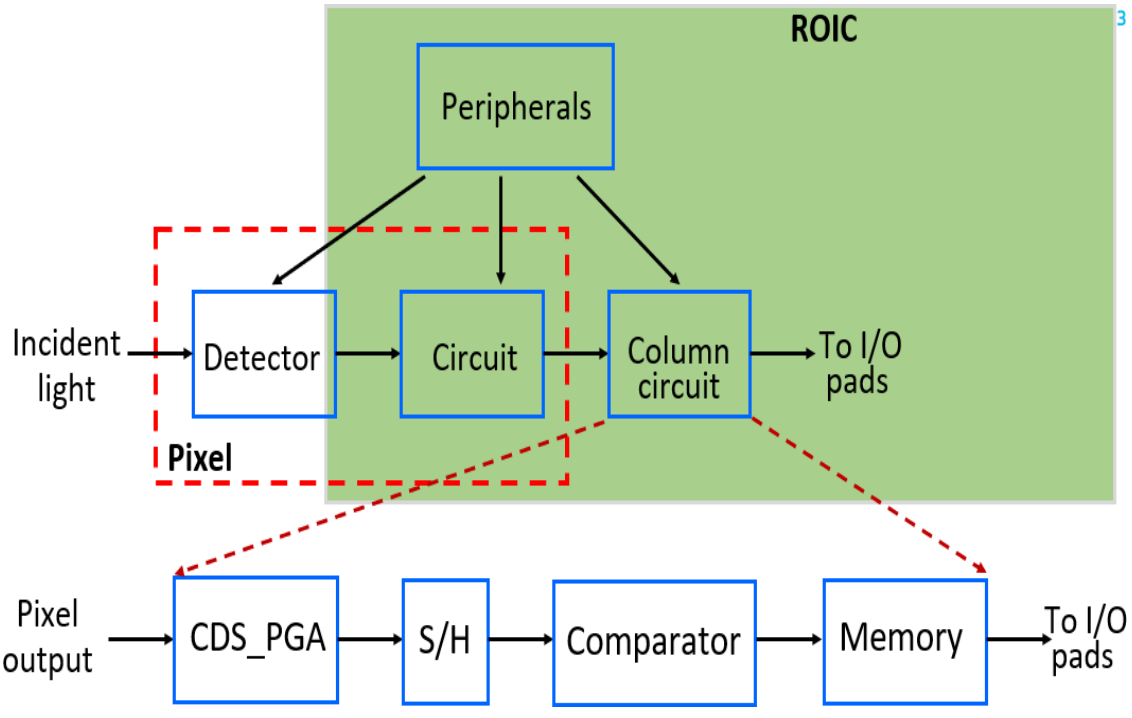

Fig 1.1 – Read Out Integrated Circuitry

During the internship, hands-on experience was gained in designing and verifying key analog building blocks utilized in the ROIC, such as operational amplifiers, buffers, current mirrors,

and analog-to-digital converters (ADCs). The design process involved exploring different topologies and configurations to optimize performance parameters like gain, bandwidth, and power consumption.

Simulation and verification were conducted using industry-standard Electronic Design Automation (EDA) tools, including Cadence Virtuoso. These simulations encompassed DC, transient, and AC analyses to evaluate the circuits' behaviour under various operating conditions. Additionally, the impact of process, voltage, and temperature (PVT) variations on circuit performance was examined to ensure robustness and reliability.

This report presents the methodologies, design approaches, simulation results, and practical implementations of the analog circuits developed during the internship, highlighting their significance in the context of CMOS image sensor technology.

1.1 Objective and Motivation

The primary objective of this internship was to provide practical experience in analog circuit design and verification, with a focus on CMOS image sensors. The work centered around the Readout Integrated Circuit (ROIC), which processes signals from the pixel array in image sensors.

This internship was chosen due to a strong interest in analog electronics and the goal of understanding how fundamental analog blocks are applied in real-world applications, such as image sensors, automotive systems, and defense technologies.

The specific tasks and areas covered during the internship included:

- Designing and analysing various analog building blocks such as operational amplifiers, current mirrors, buffers, and analog-to-digital converters (ADCs).
- Simulating and verifying the performance of these circuits using industry-standard Electronic Design Automation (EDA) tools.
- Exploring the impact of different circuit configurations and load types on the performance and behaviour of analog circuits.

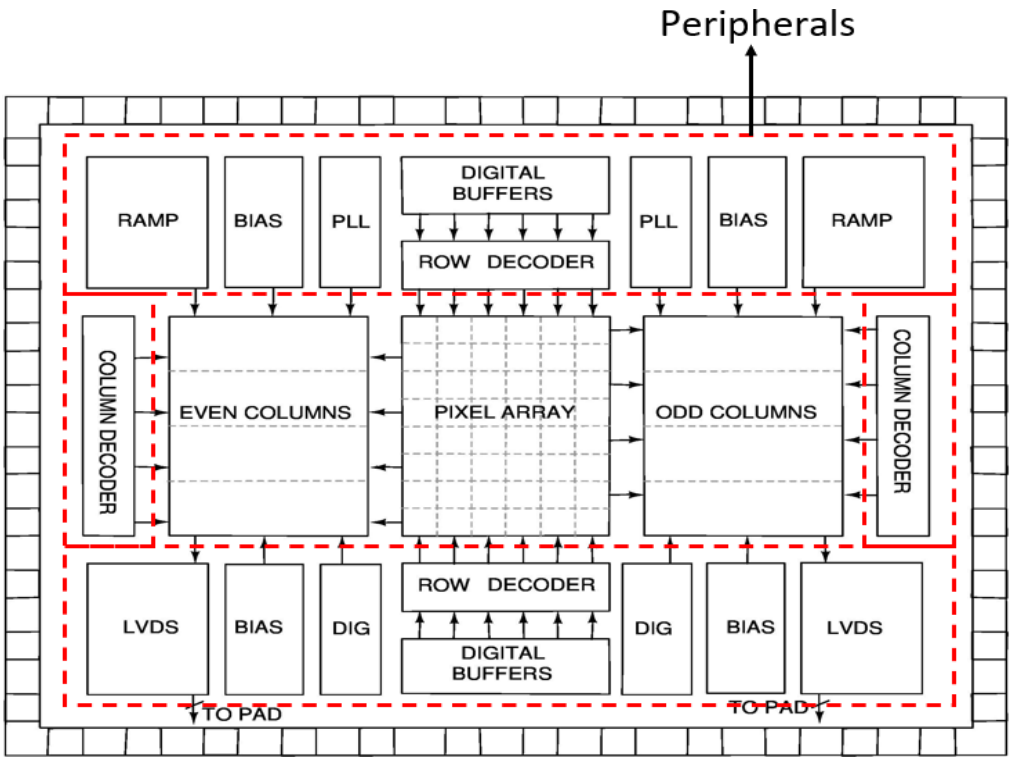

Fig – 1.2 Architecture of the CMOS Image Sensors

The core objectives of the internship were:

- To understand the operation and role of analog building blocks in CMOS image sensors.
- To design and analyze different analog circuits, including amplifiers, buffers, and ADCs.
- To verify and simulate the behaviour of these circuits using EDA tools.
- To explore how different circuit configurations impact circuit performance.

This internship provided an opportunity to apply theoretical knowledge to real-world analog circuit design tasks, while gaining hands-on experience with industry-standard tools and techniques in a professional setting.

1.2 Literature Review

High dynamic range (HDR) CMOS image sensors are essential for capturing images in varied lighting conditions. However, existing techniques to enhance dynamic range often suffer from issues like nonlinearity, high dark current noise, and inconsistent signal-to-noise ratio (SNR). A dual-transfer-gate pixel design has been developed to address these problems, achieving an 84.5 dB dynamic range in 110 nm CMOS technology with a frame rate of 76 fps in 12-bit digital format. The design incorporates correlated double sampling (CDS), reducing input noise to 3.1 electrons. Additionally, an auto-scaling ramp generator ensures 12-bit accuracy across 50 MHz to 600 MHz, offering slope adjustments from 0.112 μV/s to 1.266 μV/s for column ADCs, enabling precise and flexible signal conversion. [4]

This paper focuses on the development and evaluation of the EKV MOS transistor model for ultra-low-voltage and ultra-low-power analog IC design, using the bulk-driven technique. It extends the established compact simulation model by modifying the original parameter extraction flow. The paper includes a brief overview of the EKV model, introduces a novel parameter extraction method, and compares the developed EKV model with the BSIM v3.3 model and experimental data from prototype chips fabricated in 130 nm CMOS technology. [5]

A low-power bulk-driven (BD) OTA was developed for bio signal processing, operating at 0.5 V with 31.3 nW power consumption and a 15 nA current. Using bulk-driven and self-cascode techniques in the subthreshold region, the OTA was applied in a bandpass filter (BPF) for ECG signals, offering adjustable gain and cutoff frequency. Key metrics include −53.56 dB THD, 17.9 μVrms input noise, 75 dB CMRR, and 87.7 dB PSRR. Simulations in Cadence with TSMC 0.18 μm CMOS confirmed its suitability for ultralow-power biomedical applications.[6]

Ultra-low voltage (ULV) and ultra-low power (ULP) OTAs are crucial for energy-efficient analog designs. A ULV OTA utilizing a bulk-driven nontailed differential stage with multipath Miller zero compensation has demonstrated effective class AB operation,

achieving rail-to-rail input common-mode range. Fabricated in 180 nm CMOS, the OTA operates at 0.3–0.5 V, consuming as low as 12.6 nW at 0.3 V. It delivers a 64.7 dB voltage gain, 2.96 kHz gain-bandwidth product, and 4.15 V/ms slew rate, making it suitable for low-power applications [7]

1.3 Methodology

Analog design primarily focuses on creating circuits for processing continuous-time signals. The design process begins with creating a virtual model of the circuit, which is then tested for key parameters like voltage gain, stability, and the effects of temperature and environmental conditions. Based on the test results, adjustments are made, and the design is sent to the foundry for physical implementation on a PCB. The design undergoes further testing using software platforms like Cadence Virtuoso, LabVIEW, and Simulink. The flow from design to fabrication and PCB integration is outlined in Fig. 1. Once the circuit is completed, it is handed over to the optics team for integration with the camera system.

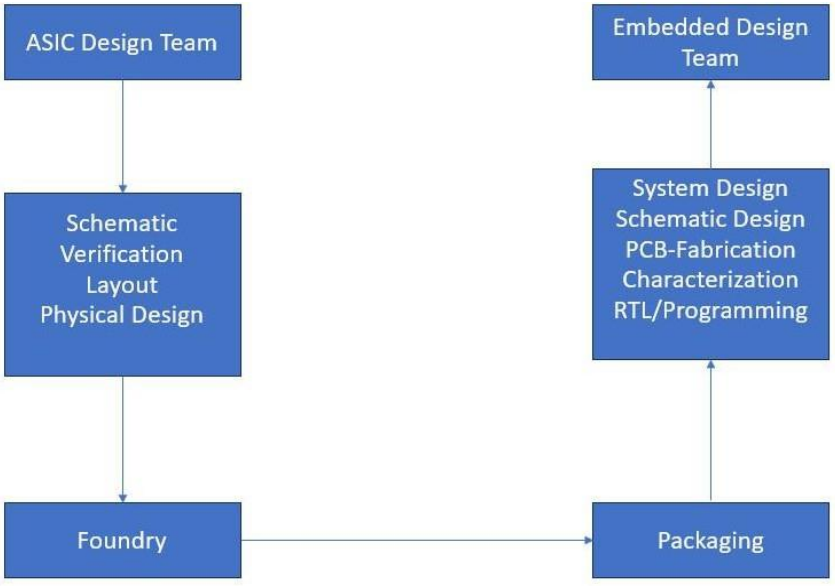

Fig 2 – Process Flow for the CMOS Image Sensors

Chapter 2

Basic ADC

TheAnalog-to-Digital Converter (ADC)

An Analog-to-Digital Converter (ADC) is an electronic device that transforms continuous analog signals into discrete digital values. This process is essential because most modern digital systems, such as microcontrollers and computers, can only process digital data, while many real-world signals (like temperature, sound, or voltage) are analog in nature.

The operation of an ADC typically involves three main steps:

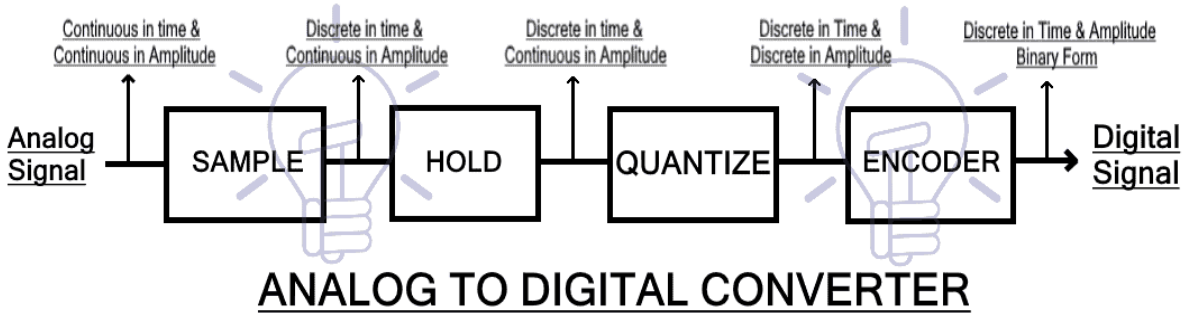

Fig 2.1 block diagram of ADC

1. **Sampling**:

   The analog signal is measured at regular intervals. These intervals are determined by the sampling rate or frequency. According to the **Nyquist theorem**, the sampling rate should be at least twice the maximum frequency present in the analog signal to accurately represent it in digital form.

2. **Quantization**:

   After sampling, each analog value is approximated to the nearest value within a finite set of levels. This process introduces a small error known as **quantization error**, but it allows the continuous range of the analog input to be represented using a limited number of discrete levels.

3. **Encoding**:

   Finally, each quantized value is converted into a binary number. The number of bits used in this binary representation determines the **resolution** of the ADC. For example, an 8-bit ADC can represent 256 (2^8) different levels.

Key Characteristics of ADCs

- **Resolution**: Indicates how finely the analog signal is divided. Higher resolution means better detail in representing the input signal.
- **Sampling Rate**: The number of samples taken per second, measured in samples per second (S/s or Hz).
- **Accuracy**: How close the output digital value is to the actual analog input.
- **Input Range**: The range of analog voltages the ADC can convert (e.g., 0–5V).

2.1 Types of ADCs

1.SAR ADC
2.Flash ADC
3.Sigma/Delta (ΔΣ) ADC
4.Dual slope ADC

2.1.1 SAR ADC

A Successive Approximation Register (SAR) ADC converts an analog input signal into a digital output through an iterative process that refines the estimate of the input voltage step by step. The core idea is based on binary search logic, where the ADC successively narrows down the range within which the input voltage lies.

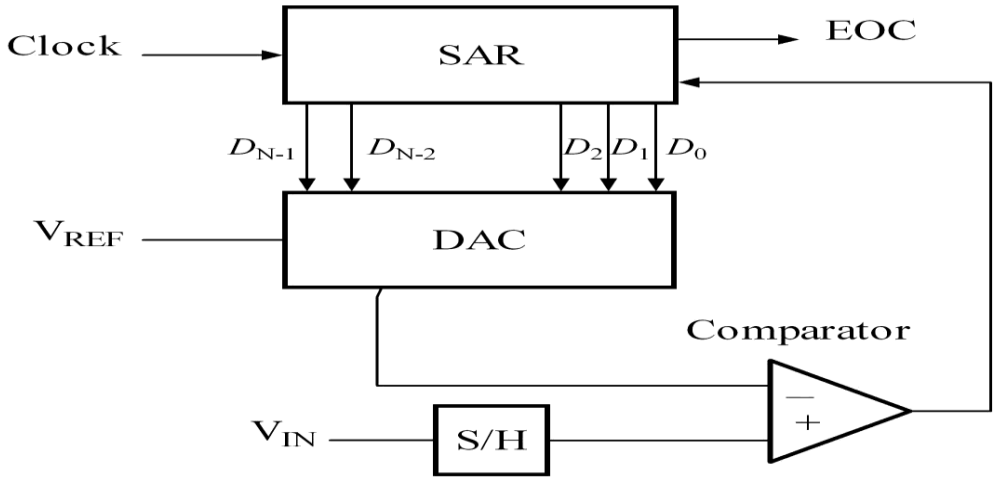

Fig 2.2 Block diagram of SAR ADC

2.1.2 FLASH ADC

A Flash ADC, also known as a parallel ADC, is one of the fastest types of analog-to-digital converters. It operates by using a large number of comparators, each one comparing the input voltage to a unique reference voltage.

Basic Working Principle

The input analog voltage is simultaneously fed into all the comparators. Each comparator has a different reference voltage, typically generated using a resistor ladder connected between a reference high voltage and ground. When the input voltage exceeds the reference voltage of a given comparator, that comparator outputs a logic high (1); otherwise, it outputs a logic low (0).

As a result, for any given input voltage, several comparators will output '1', and the rest will output '0'. The output pattern of the comparators forms what is known as a thermometer code — a sequence of ones followed by zeros. A digital encoder then converts this thermometer code into a binary number that represents the digital equivalent of the input analog voltage.

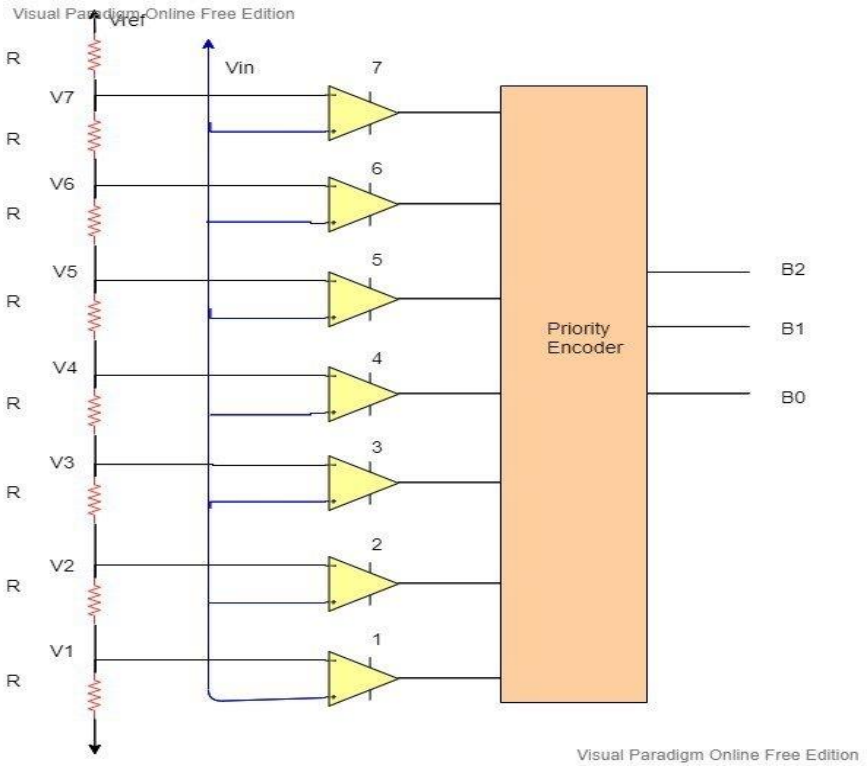

Fig 2.3 Flash type ADC Block diagram

Chapter 3

Current Mirrors

A current mirror is a critical analog circuit component designed to accurately copy a reference current to one or more output branches. It serves as an essential biasing tool for MOSFETs in analog integrated circuits. Compared to resistor-based biasing approaches—which suffer from significant variations due to manufacturing tolerances, supply voltage fluctuations, and temperature changes—current mirrors provide far greater stability and precision. This robustness against PVT (Process, Voltage, Temperature) variations makes them indispensable in modern IC design.

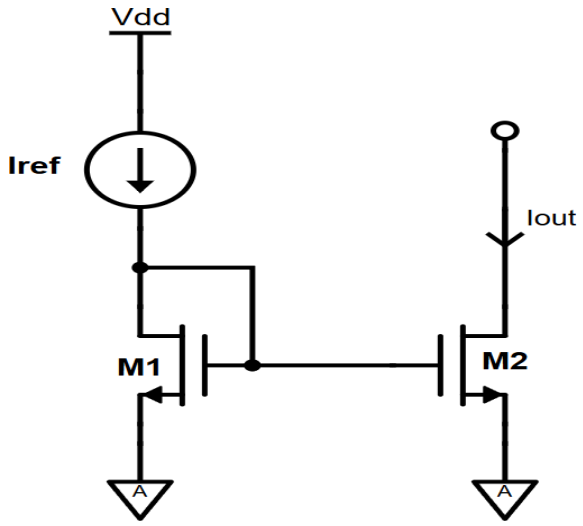

Fig 3.1 Current Mirror Circuit

The Output Current will be :

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} I_{ref} \qquad (3.1)$$

The **simple current mirror** works well but suffers from the following drawbacks:

1. Low Output Resistance
2. Reduced Accuracy
3. Limited Output Swing

Different Configurations of Current Mirrors are

- Cascode current mirror
- Wide Swing Cascode current Mirror.
- Wilson current Mirror.

Structure of High Swing Current Mirror

A wide swing current mirror typically builds on the **cascode current mirror** by employing a modified cascode structure or **adaptive biasing** to reduce the required voltage headroom.

1. Basic Transistor Pair
2. Modified Cascode Transistors
3. Adaptive Biasing
4. High Output Resistance

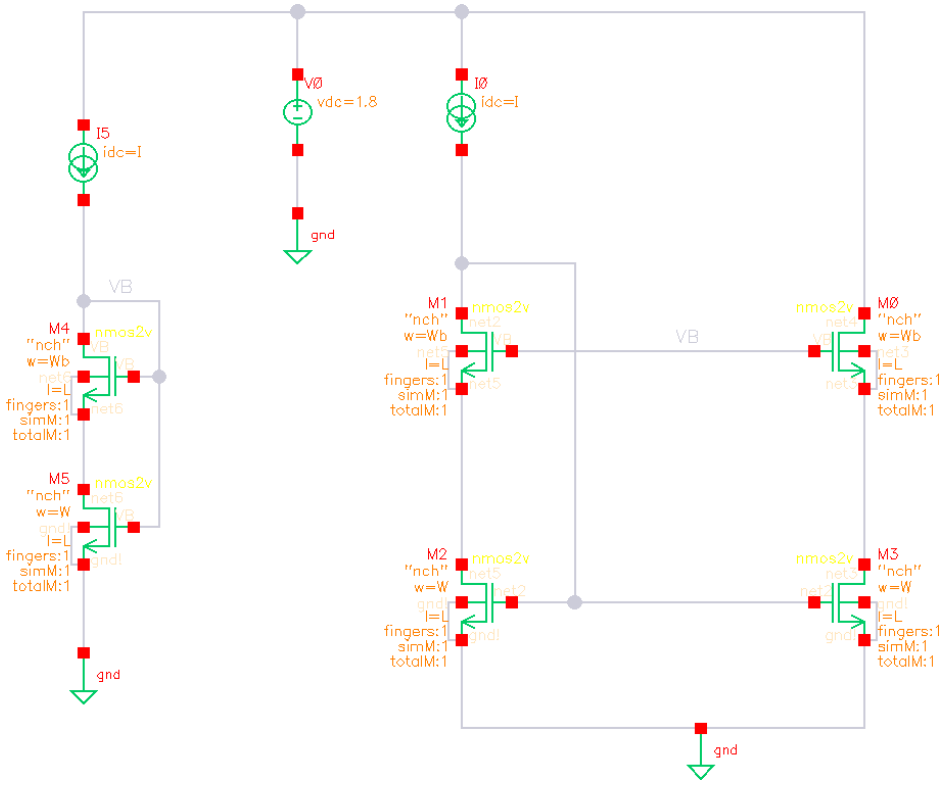

Figure 3.2: Schematic of High Swing Cascode Current Mirror.

Chapter – 4

Differential and Operational Amplifiers Configurations

4.1 Differential Amplifier with Resistive Load

The differential amplifier is a fundamental circuit that selectively amplifies the voltage difference between its two input terminals while effectively suppressing identical signals (common-mode voltages) present at both inputs. This dual functionality enables precise extraction and amplification of small differential signals even in the presence of large common-mode interference.

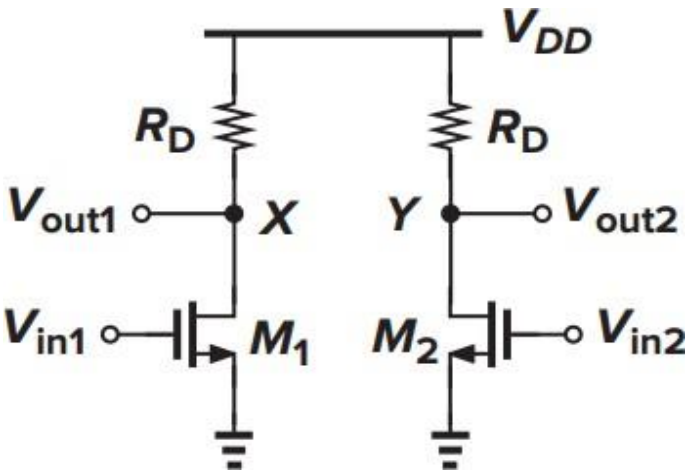

Figure 7.1: Differential Amplifier with Resistive Load.

Working Principle

The output voltage (V_{out}) is proportional to the difference between the two input voltages (V_1 and V_2):

$$\mathbf{V_{out} = A_d * (V_1 - V_2)} \qquad \mathbf{(4.1)}$$

where:

- A_d: Differential gain (amplification of the voltage difference).
- V_1, V_2: Input voltages.

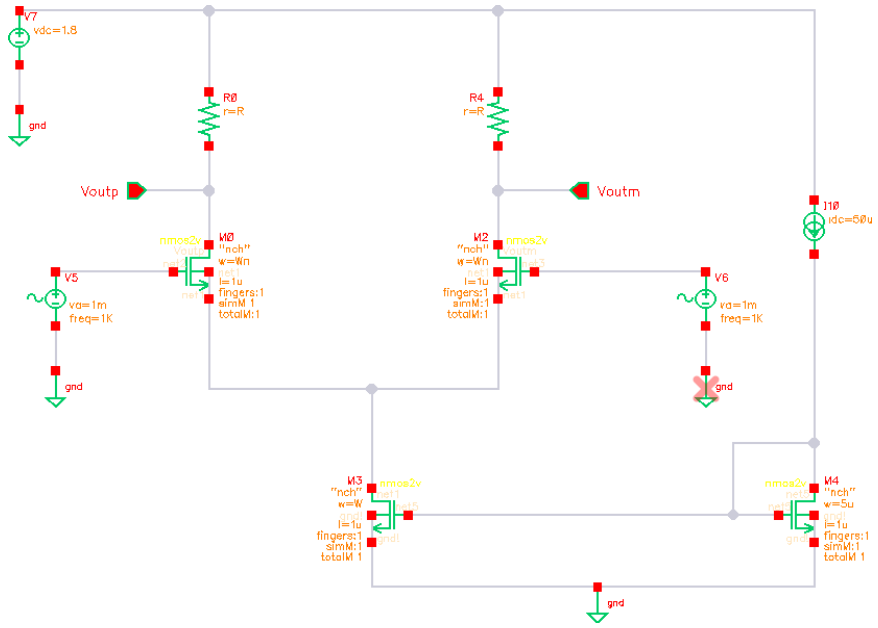

Fig 4.2: Testbench for Diff Amp with Resistive Load

The amplifier suppresses the common-mode voltage (V_{cm}), defined as:

$$\mathbf{V_{cm}} = \frac{V_1 \pm V_2}{2} \tag{4.2}$$

The Input Common Mode range for the Diff Amp will be :

$$\boldsymbol{ICMR} = 2V_{OV} + V_{TH}\ To\ VDD - I_{D/2} * R_D + V_{TH} \tag{4.3}$$

The Output Common Mode Range for the Diff Amp is

$$\boldsymbol{OCMR} = 2V_{OV}\ To\ VDD - I_{D/2} * R_D \tag{4.4}$$

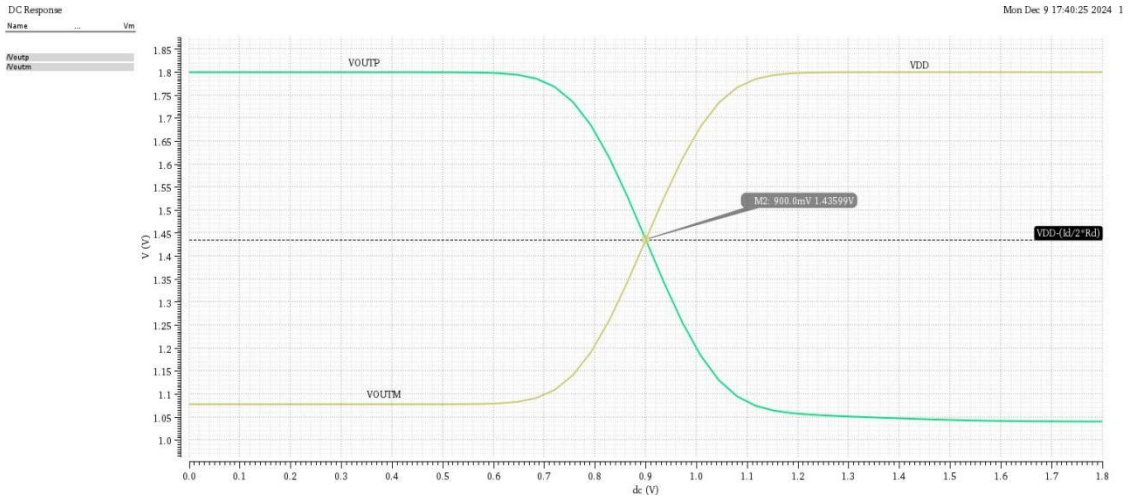

Fig – 4.3 Output Voltages V/s (V_{in1}-V_{in2})

Key Parameters

1. ***Differential Gain (A_d):*** Amplifies the voltage difference between inputs.
2. ***Common-Mode Rejection Ratio (CMRR):*** Measures the ability to reject common-mode signals.

$$\textbf{CMRR (in dB)} = 20 * log_{10} \frac{A_d}{A_{cm}}$$

Higher CMRR indicates better performance.

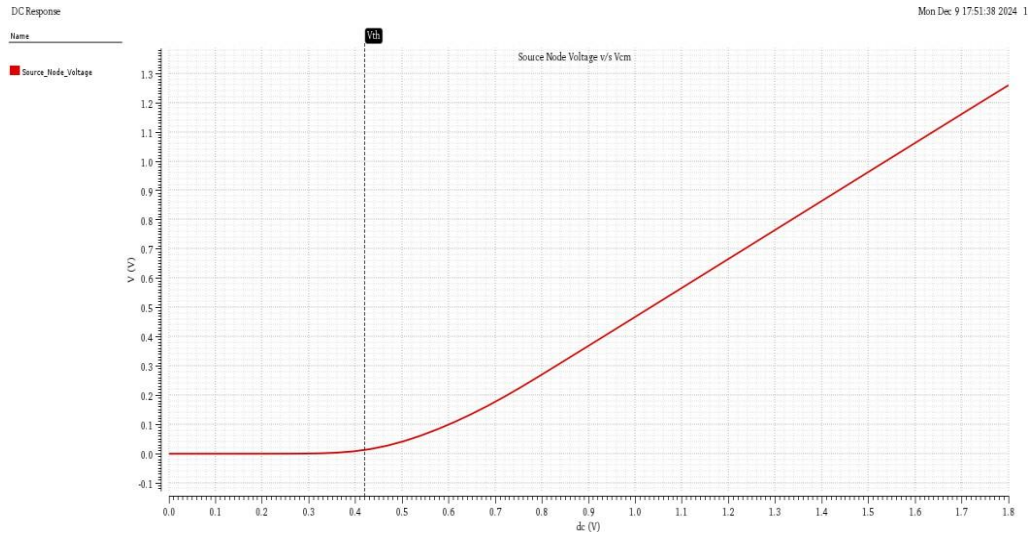

Fig – 7.6 Source node Voltage v/s Common mode Voltage

As the input voltage increases, the source potential tends to follow due to the behavior of the differential pair and the tail current source, which together resemble a source follower configuration. To maintain equal currents through both transistors, their gate-to-source voltage Vgs must remain the same. As a result, any additional voltage appears as a drop across the tail node .

Advantages of Differential Amplifiers

- Excellent noise immunity (rejects common-mode signals).
- Amplifies small differential signals.
- Can be designed for precise gain and bandwidth.

4.2 Operational Transconductance Amplifier (5-OTA)

A (5-OTA) is a voltage-controlled current source that functions as a differential amplifier with an active load. It is primarily used for converting differential input signals to a single-ended output, where the output is represented as a current. This configuration is recognized as a transconductance stage because it accepts differential voltage inputs and provides a proportional current output. The 5-OTA is a stable circuit, well-suited for driving capacitive loads, as it effectively maintains the desired gain and ensures the proper operating region of the MOS transistors.

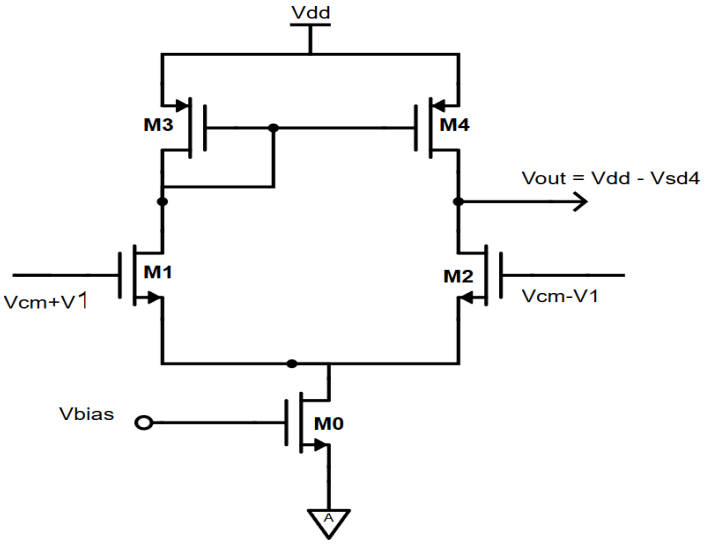

Fig – 5 Transistor OTA

The Input Common Mode range is given by:

$$ICMR = (V_{OV1} + V_{OV0} + V_{TH}) \; To \; (VDD - V_{SG3} + V_{TH}) \quad (4.5)$$

The Output Common Mode Range is given by:

$$OCMR = (V_{OV2} + V_{OV0}) \; To \; (VDD - V_{SD4}) \quad (4.6)$$

As from equ 4.6 we can see that our signal can't archive rail to rail swing that is one of the drawbacks for the OTA to mitigate that we have to include a class AB amplifier to maintain that swing.

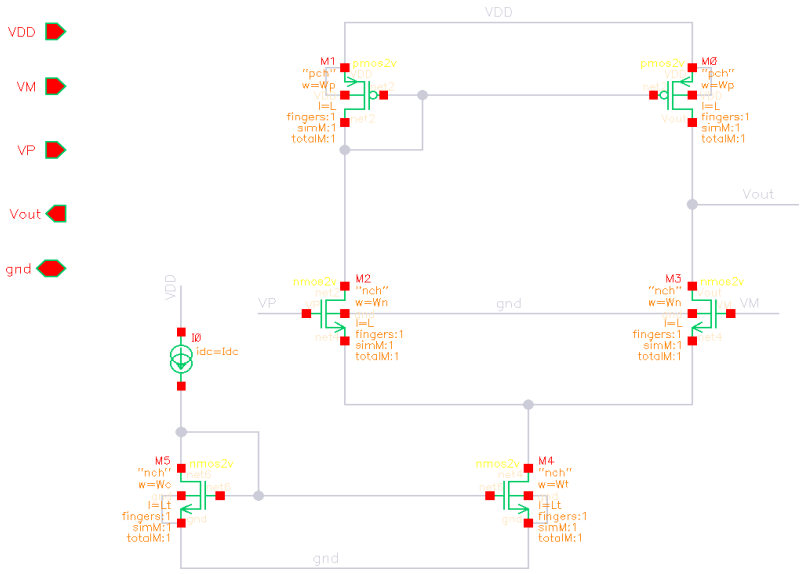

Fig 4.2 Schematic of 5 OTA

Design Specification for the OTA is:

VDD = 1.8, gain = 50dB, TSMC – 180nm , GBW =10 MHz ,CL – 1pF , ICMR- = 0.8 V , ICMR+ = 1.2 V , V_{OV} = 0.2 V

Table 2 – Aspect ratios for OTA

Parameters	**Values**
IDC	10µA
(W/L) of M4 & M5	(1.5µm/ 0.8µm)
(W/L) of M2 & M3	(2.5µm / 0.8µm)
(W/L) of M1 & M0	(3µm / 0.8µm)

The OTA is rarely used in open loop configuration although it is stable, and for load we won't use resistor because it changes the operating region of the circuit and also the output impedance which eventually decreases the gain.

4.2.1 Large Signal Analysis of 5T Operational Transconductance Amplifier

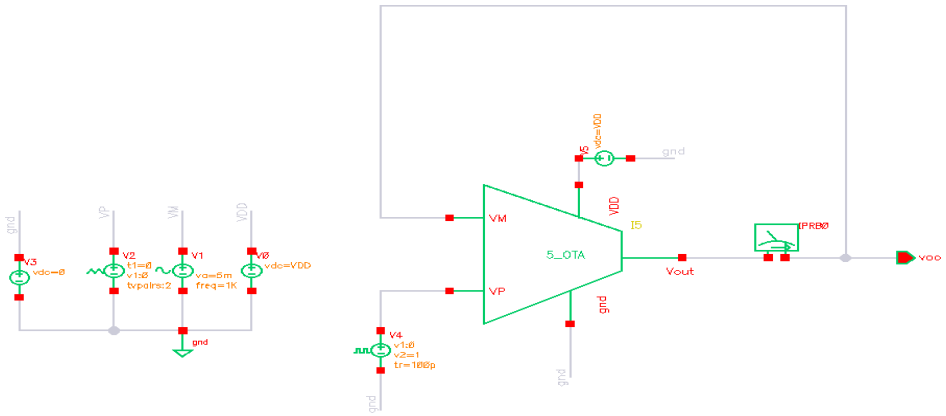

Fig 4.3 – Testbench Setup for 5-OTA

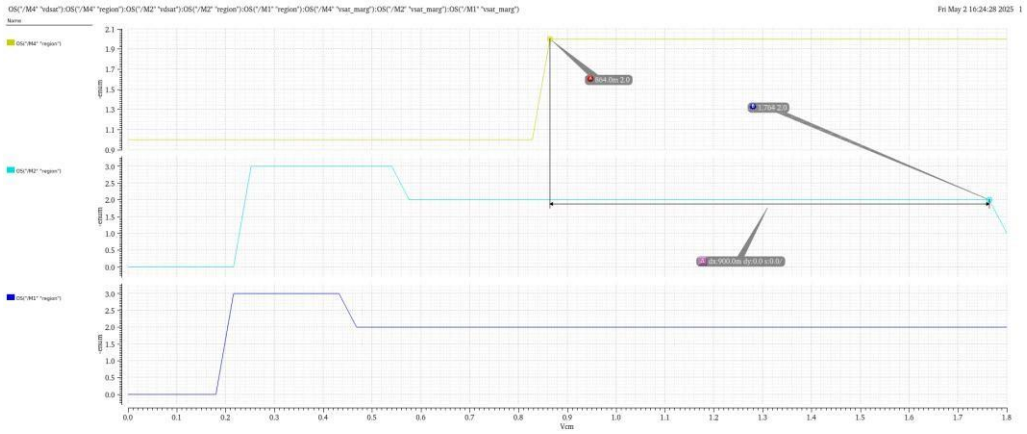

Fig 4.5 – ICMR range for the 5-OTA (900mV)

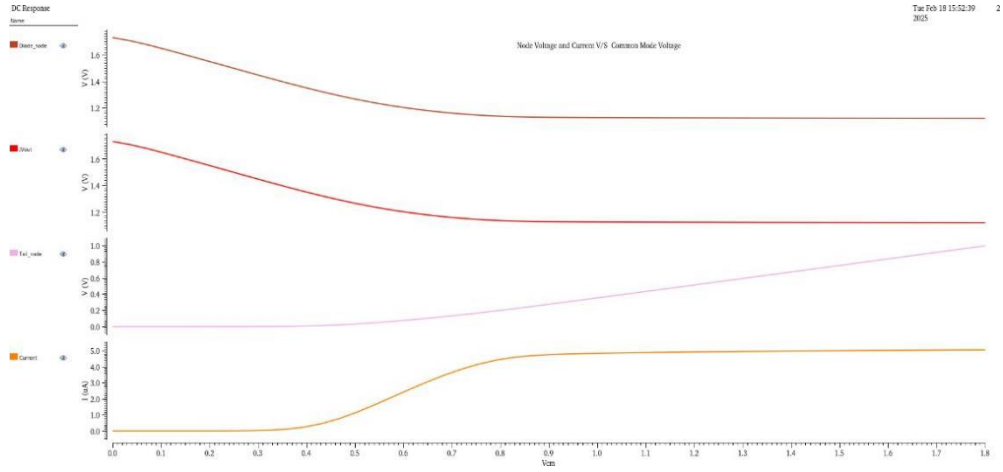

Fig 4.6 – Node Voltage and Current v/s Vcm

From the (fig 4.6), as the common-mode voltage (Vcm) increases, the tail node voltage follows Vcm to maintain a constant branch current. This results in an increased voltage drop at the tail node. For the differential pair operating in a common-source (CS) configuration, an increase in Vcm causes a reduction in the drain voltage. Given that the PMOS current mirror must maintain the same branch current, the decrease in drain voltage leads to an increase in the source-gate voltage of the PMOS devices, effectively compensating for the variation and preserving the overall current balance within the circuit.

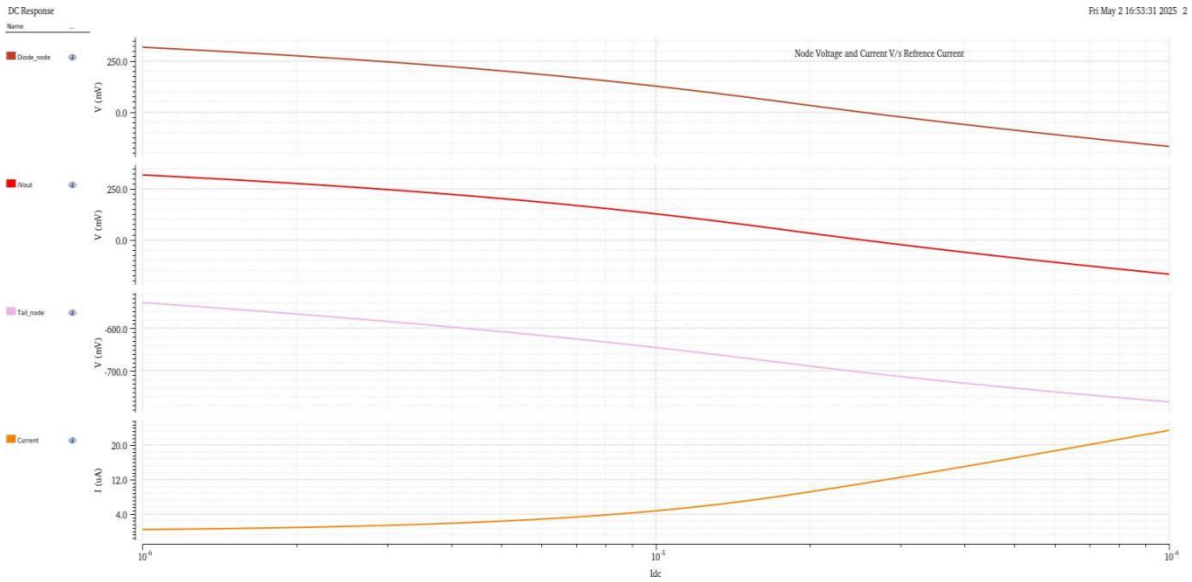

Fig 4.7 – Node voltage and current v/s I_{DC}

From the above (Fig 4.7) we analyse that, increase in the tail current directly leads to a proportional increase in the branch currents of the differential pair, assuming all other parameters remain constant. To accommodate this increased current, the tail node voltage and the drain voltages of the differential pair transistors decrease. This reduction in node voltages results in a corresponding increase in the gate-source voltage of the NMOS transistors and the source-gate voltage of the PMOS transistors in the current mirror, with the magnitude of these voltage changes directly reflecting the increase in current.

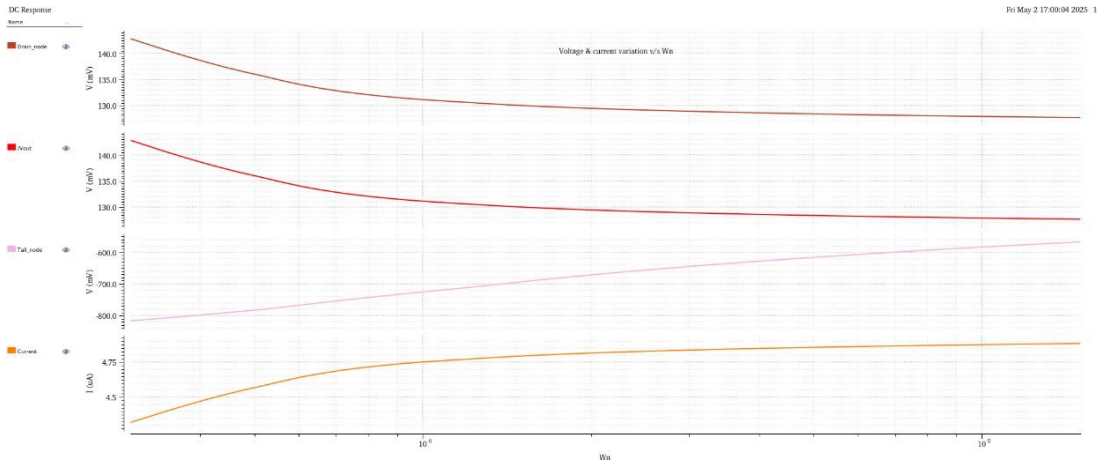

Fig 4.10 – Node voltage and current variation w.r.t width of NMOS diff pair

As depicted in Fig 4.10, increasing the width of the NMOS transistors in the differential pair of the 5-OTA configuration reduces their overdrive voltage , assuming the same current must be maintained in both branches. This reduction in Vov leads to a decrease in the required gate-source voltage for the NMOS transistors. Consequently, the tail node voltage increases to accommodate the reduced overdrive. Simultaneously, the drain voltages of the PMOS transistors decrease, resulting in an increase in the source-gate voltage of the PMOS current mirror. This adjustment effectively compensates for the reduced NMOS overdrive, ensuring that the branch currents remain balanced.

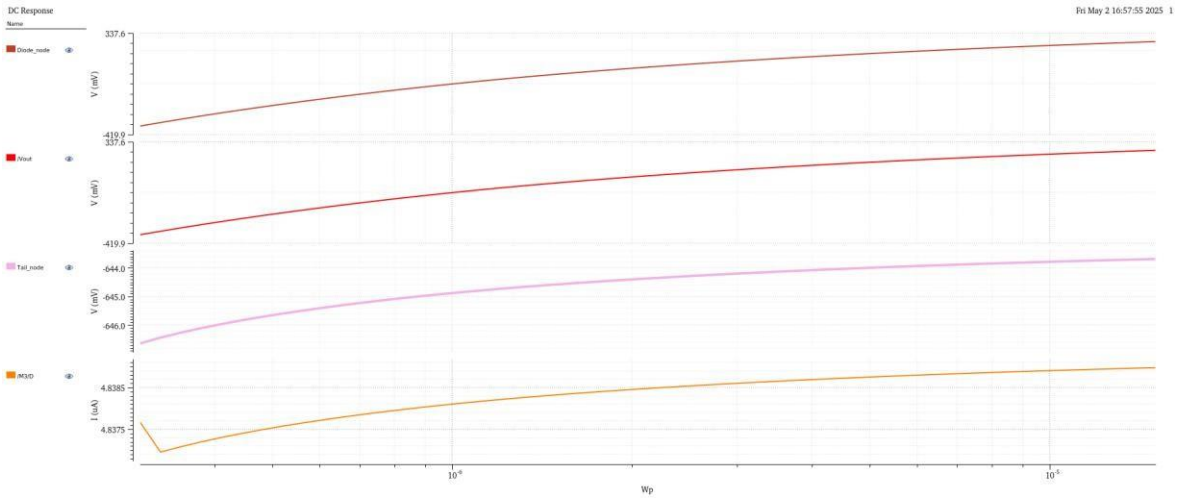

Fig 4.11 – Node voltage and current variation w.r.t width of PMOS

4.2.2 Small Signal Analysis 5T Operational Transconductance Amplifier

For the small-signal analysis of the 5-OTA configuration, leveraging the half-circuit concept significantly simplifies the analysis. This approach is valid if the output resistance of transistor M2 is sufficiently high, ensuring that the impedance seen from both branches is identical. Under this condition, the differential pair can be considered to operate under a virtual short-circuit condition at the common-source tail node.

So for that the short circuit transconductance is given by :

$$G_m = \frac{I_{out}}{V_1 - V_2} = g_{m1,2} \tag{4.7}$$

And the output impedance is given by :

$$R_{out} = r_{op} || r_{on} \tag{4.8}$$

Now the small signal voltage gain is given by ,

$$A_v = -G_m * R_{out} \tag{4.9}$$

$$A_v = -g_{m1,2} * (r_{op} || r_{on}) \tag{4.10}$$

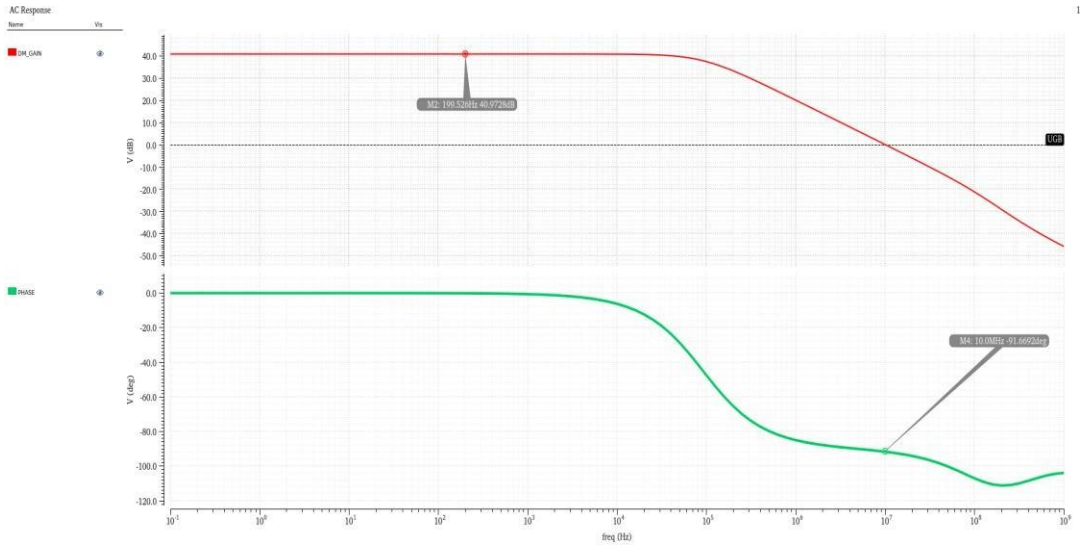

Fig – 4.12 gain & phase plot v/s frequency for OTA

Some key parameters for the analysis of OTA will be CMRR and PSRR,

1. ***Common-Mode Rejection Ratio (CMRR):*** Measures the ability to reject common-mode signals.

$$\textbf{CMRR (in dB)} = 20*log_{10}\frac{A_d}{A_{cm}} \qquad \textbf{(4.11)}$$

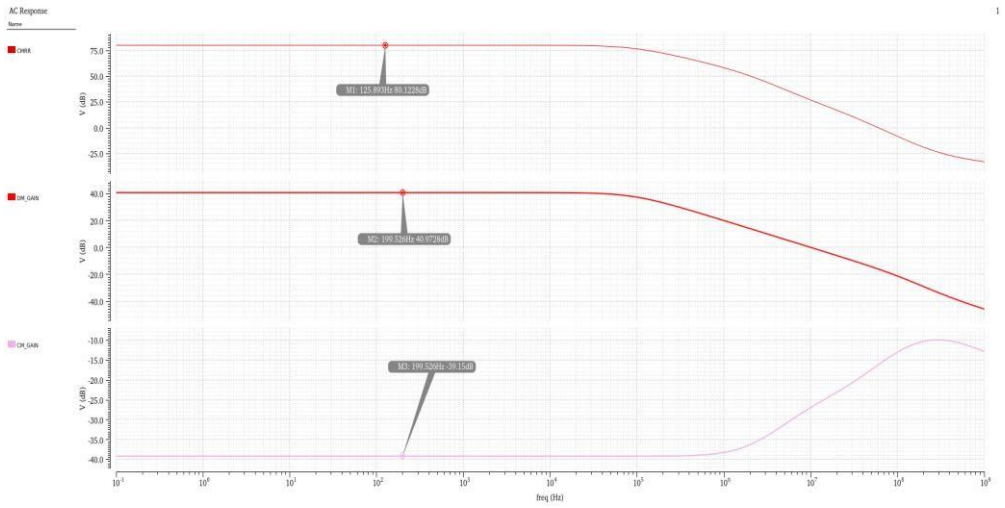

Fig 4.13 – Common mode rejection ratio of 5OTA

2. ***Power Supply Rejection Ratio (PSRR)*** : It is defined as how effectively a circuit maintains stable output voltage despite fluctuations in its input power supply .

$$PSRR = 20 * log_{10}\frac{A_{dm}}{A_{power}} \qquad (4.12)$$

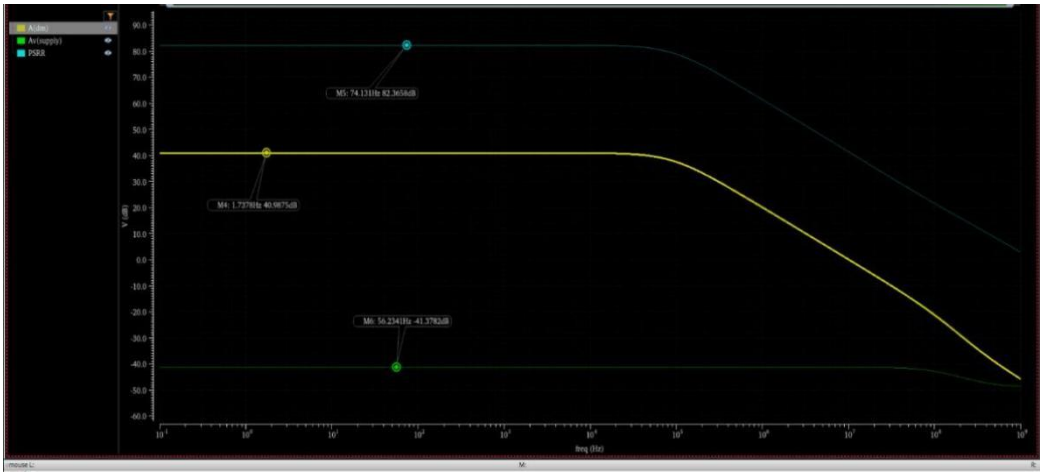

Fig 4.14 – PSRR of OTA

4.3 Telescopic Cascode Amplifier

In a conventional 5-OTA, the gain is limited and eventually saturates. To enhance the gain, either the transconductance (gm) can be increased, or the output impedance can be enhanced. The more practical approach is to increase the impedance using cascode transistors, leading to the Telescopic Cascode Amplifier. This structure boosts gain by cascoding transistors, but it introduces challenges such as reduced output swing, additional poles, and stability issues due to a mirror pole. Its high output impedance also complicates input-output shorting, making it unsuitable for unity-gain buffer applications.

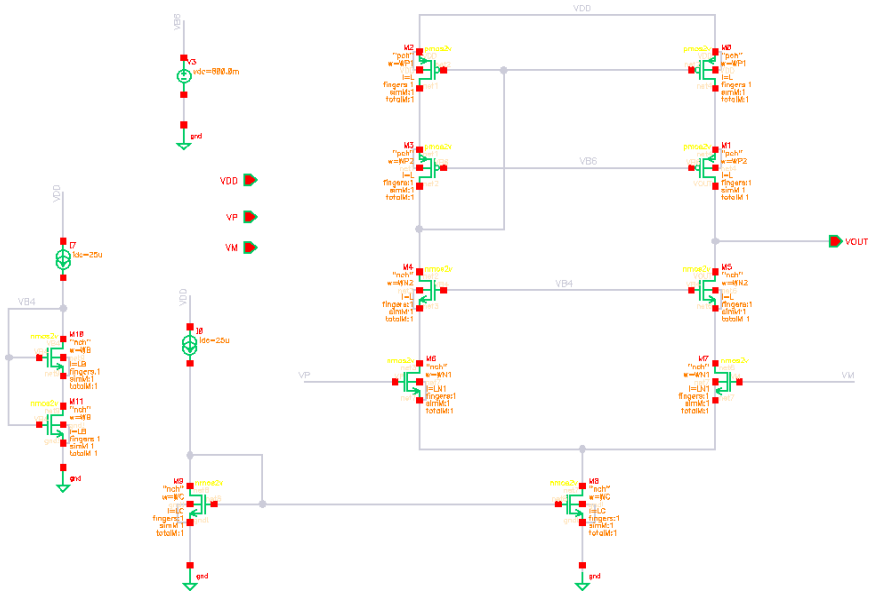

Fig 4.15 Telescopic Cascoded Amplifier

The input common mode range is given by:

$$ICMR = V_{OV6} + V_{OV6} + V_{TH} \; To \; V_{B4} - V_{GS4} + V_{TH2} \qquad (4.13)$$

The output common mode range is given by :

$$OCMR = V_{OV5} + V_{OV7} + V_{OV8} \quad To \; V_{DD} - V_{SD8} - V_{GS6} + V_{TH} \qquad (4.14)$$

To bias the circuitry and to enhance the gain we had used here some self-biased circuit mainly high swing cascode current mirror such that to maintain high gain and swing.

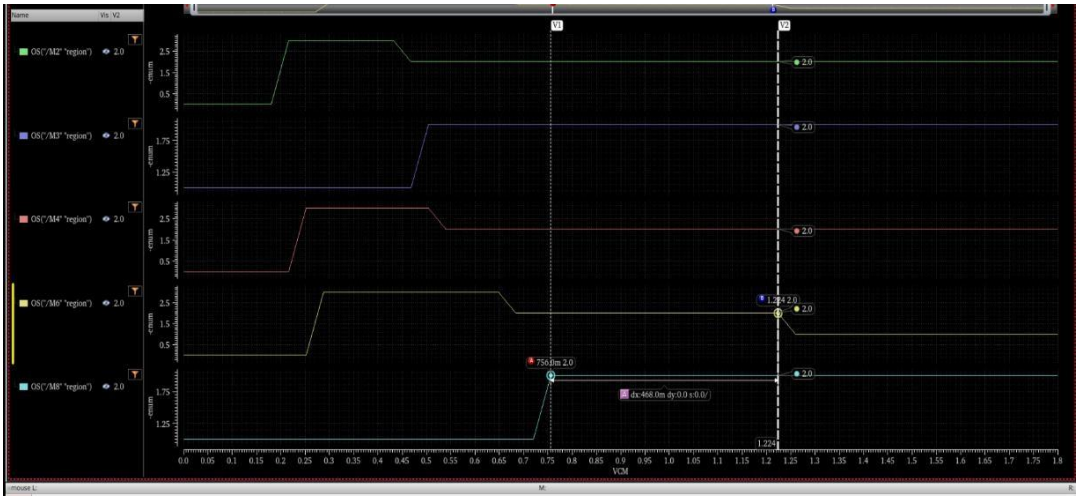

Fig 4.16 ICMR Range of Telescopic Cascode Amplifier

So for that the short circuit transconductance is given by :

$$G_m = \frac{I_{out}}{V_1 - V_2} = g_{m8,7} \tag{4.16}$$

And the output impedance is given by :

$$R_{out} = g_{m6} r_{06} r_{o8} || g_{m4} r_{04} r_{o2} \tag{4.17}$$

Now the small signal voltage gain is given by ,

$$A_v = -G_m * R_{out} \tag{4.18}$$

$$\boldsymbol{A_v = - \ g_{m8,7} * (g_{m6} r_{06} r_{o8} || g_{m4} r_{04} r_{o2})} \tag{4.19}$$

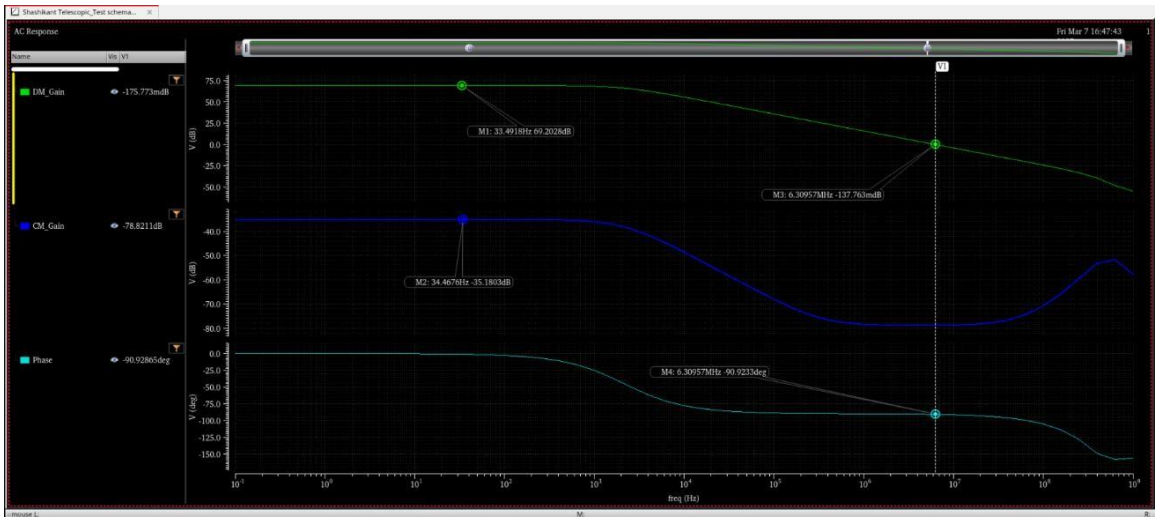

Fig 4.17 – Gain & Phase plot for Telescopic Cascode

Design Specification for the telescopic Cascode Amplifier is:

TSMC = 180nm , VDD = 1.8 V, Gain – 60dB, Slew rate = 5 $V/\mu S$, GBW = 10 MHz ,CL =5pF , ICMR- = 0.8 V ,ICMR+ = 1.2 V.

Table 03 Aspect ratios for Telescopic Cascode

Parameters	Values
(W/L) of M8 & M9	(3µm/ 1µm)
(W/L) of M0 & M2	(3µm/ 0.6µm)
(W/L) of M1 & M3	(3µm / 0.6µm)
(W/L) of M4 & M5	(3µm / 0.6µm)
(W/L) of M6 & M7	(12µm / 0.8µm)

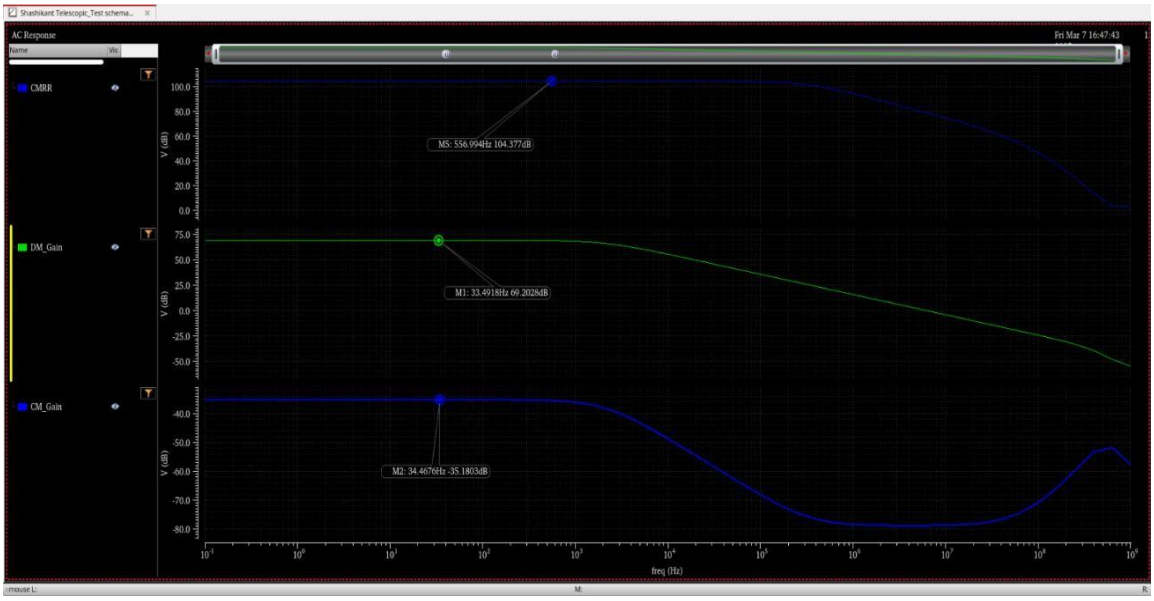

Fig 4.18 – Common Mode Rejection Ratio (CMRR) for the Telescopic Cascode

4.4 Folded Cascode Amplifier

It is an operational amplifier design that offers a high gain and wide output swing, making it suitable for deep negative feedback applications. Unlike traditional telescopic amplifiers, which have limited output swing due to their stacked transistors, folded cascode amplifiers provide a larger output swing by folding the current from one type of transistor (NMOS) to another (PMOS) or vice versa.this amplifier has reduced coupling between ICMR and OCMR, allowing the input to vary from 0V to VDD depending on the configuration.

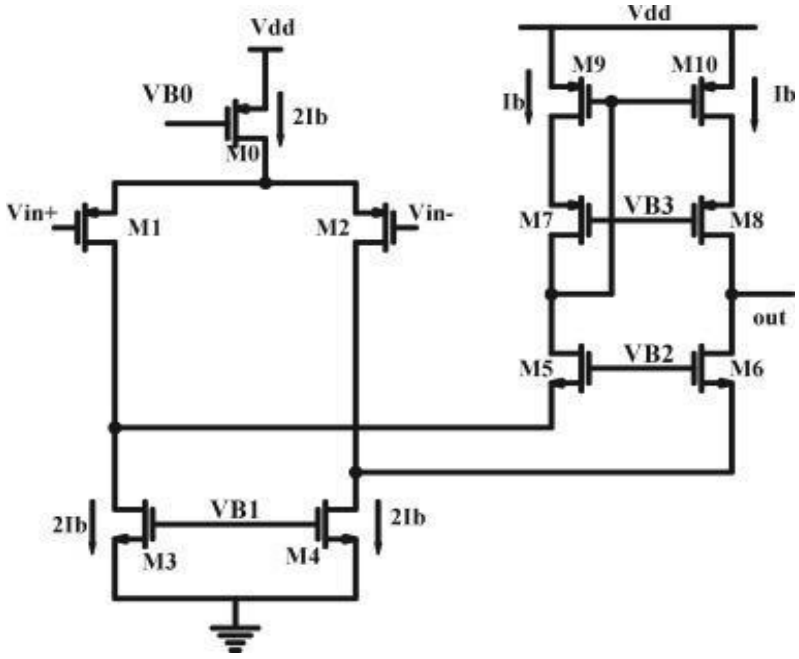

Fig 4.19 – Folded Cascode Amplifier

It has two current paths, reduces transistor stacking, and allows input and output to be shorted together.

The Input Common Mode range for the proper working will be given as:

$$\boldsymbol{ICMR} = V_{B2} - V_{GS6} - |V_{TH}| \;\; To\, VDD - V_{OV21} - V_{OV2} - |V_{TH}| \qquad (4.20)$$

The Output Common Mode range will be :

$$\boldsymbol{OCMR} = V_{OV4} + V_{OV6} \;\; To\, VDD - V_{OV10} - V_{OV8} \qquad (4.21)$$

So for that the short circuit transconductance is given by :

$$G_m = \frac{I_{out}}{V_1 - V_2} = g_{m1,2} \qquad (4.22)$$

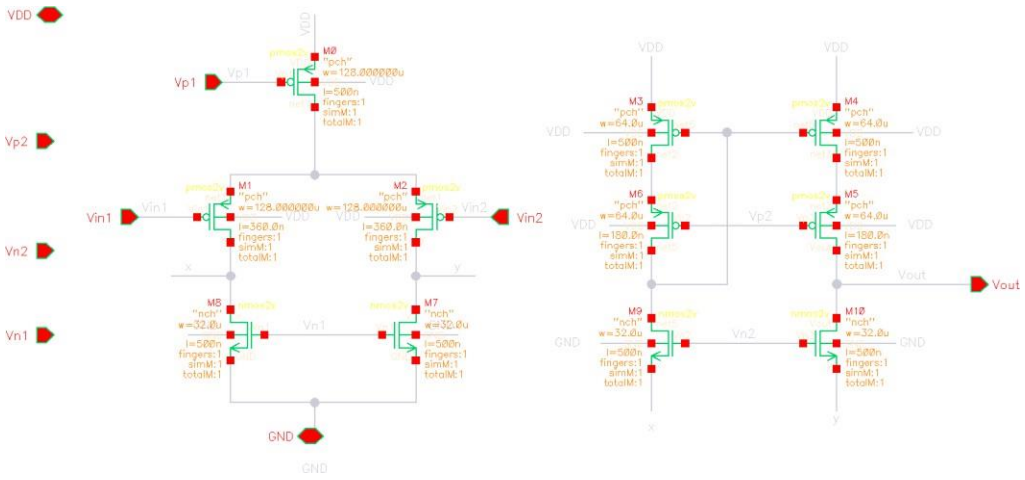

Fig 4.20 – Schematic for the PMOS based folded cascoded Amplifier

And the output impedance is given by :

$$R_{out} = \quad g_{m6}r_{06}r_{o8}||g_{m4}r_{04}r_{o2} \tag{4.23}$$

Now the small signal voltage gain is given by ,

$$A_v = -G_m * R_{out} \tag{4.24}$$

$$\boldsymbol{A_v = - \quad g_{m1,2} * (g_{m8}r_{08}r_{o10}||g_{m6}(r_{04}||r_{o2})r_{o6})} \tag{4.25}$$

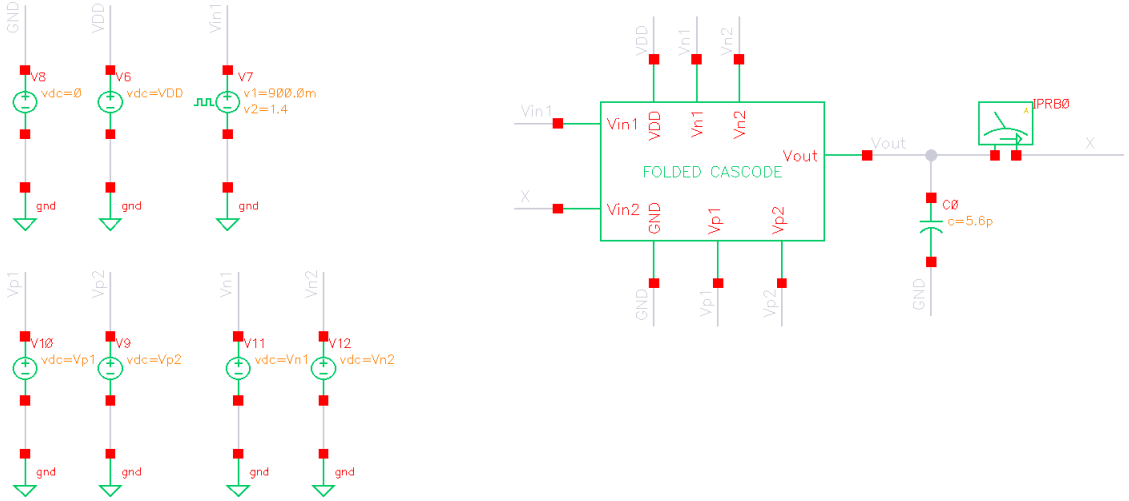

Fig 4.21 – Testbench Setup for the Analysis of the folded Cascode

4.4 Two – Stage Operational Transconductance Amplifier

Single-stage amplifiers typically involve a trade-off between gain and output swing range. In contrast, multi-stage amplifiers can achieve higher gain without significantly compromising the swing range. However, the primary challenge with multi-stage amplifiers is ensuring sufficient phase margin to maintain stability, especially when configured in feedback mode.

One effective approach to enhance gain and maintain an acceptable swing range is through cascading, where the overall gain is a product of the gains of successive stages. This method not only amplifies the signal more effectively but also provides better control over the output swing.

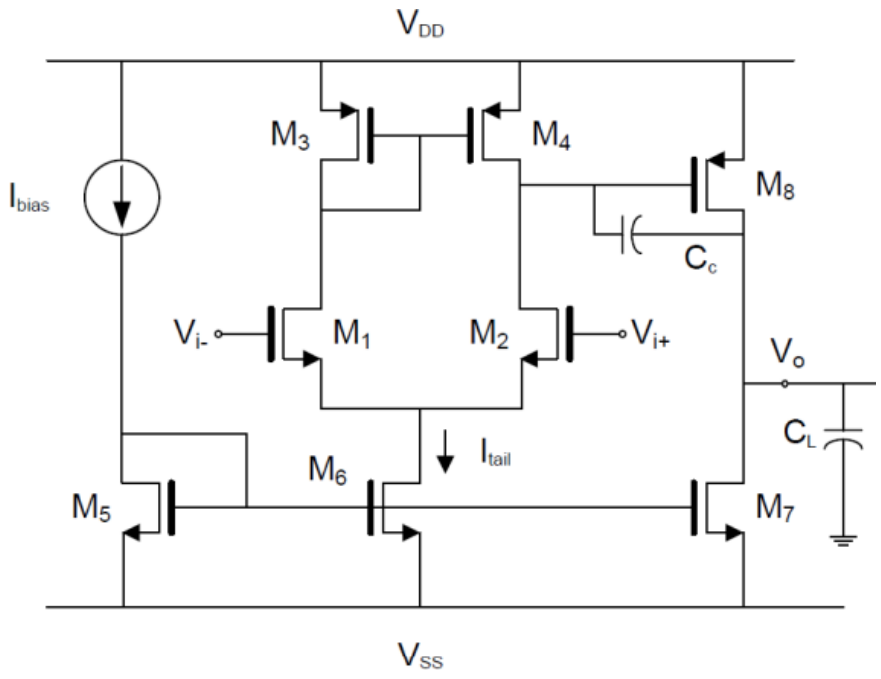

Fig 4.22 – Two stage Operational transconductance Amplifier

A common example of a multi-stage amplifier is the two-stage operational amplifier (op-amp). The first stage typically consists of a basic five-transistor operational transconductance amplifier (OTA), which is followed by a common-source stage. However, due to the presence of the Class AB output stage, this configuration can be prone to instability if not properly stabilized in feedback mode. Careful compensation techniques must be employed to ensure a stable and reliable operation.

In two-stage operational transconductance amplifiers (OTAs), the order of the system increases due to the introduction of additional poles, which can lead to instability and signal attenuation. To address these issues, the Miller compensation technique is commonly employed. This method involves introducing a dominant compensation capacitor between the first and second stages. This capacitor effectively separates the poles, ensuring that only one dominant pole is present before the unity-gain bandwidth (UGB), making the system behave like a single-pole system within this frequency range.

In some designs, a resistor is added in series with the compensation capacitor to further enhance phase margin. This configuration enables pole-zero cancellation, where a right-half-plane (RHP) zero is introduced to counteract an unwanted pole, improving the system's stability. These techniques are crucial for maintaining stability and achieving the desired phase margin in two-stage OTAs.

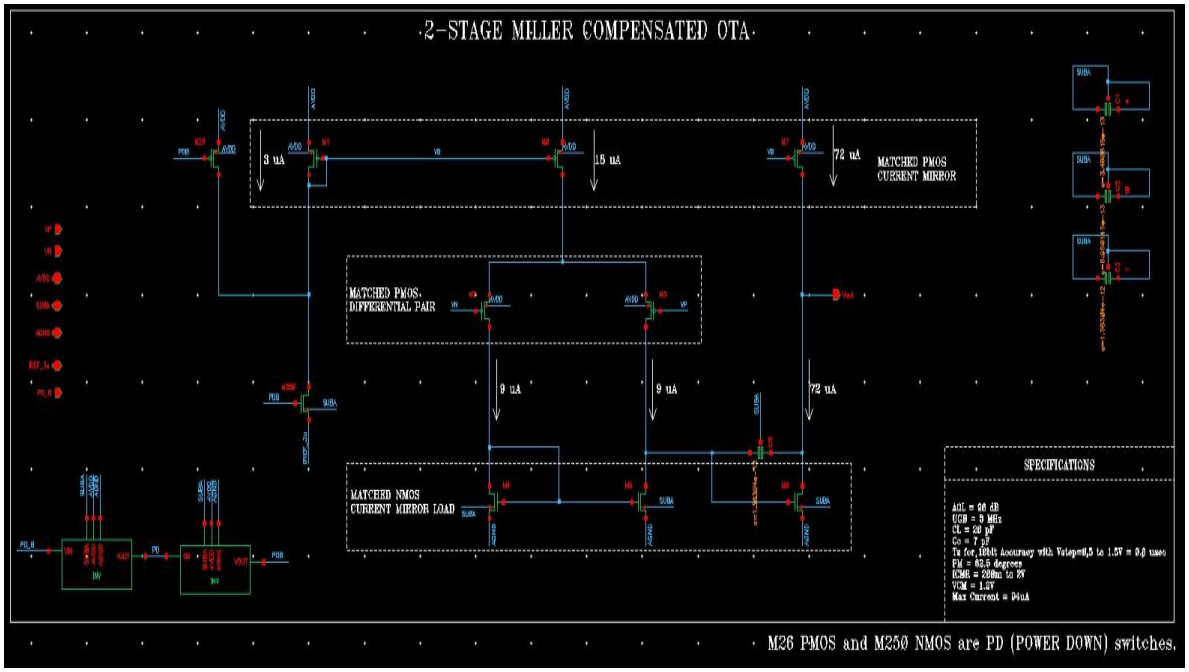

Fig 4.23 – PMOS based 2 stage OTA for BIDESA Project

For my internship, I have been assigned the task of verifying the reference buffer (Vref_buffer) for the ST40 technology node. This involves conducting both pre-layout and post-layout simulations and analysing the corresponding results for the circuit. This buffer is designed using a PMOS configuration with power-up and power-down control for the BIDESA project.

The Input Common Mode Range for fig 4.22 is given by:

$$\boldsymbol{ICMR} = V_{OV6} + V_{OV1} + V_{TH}\ To\ VDD - V_{SG3} + V_{TH} \quad (4.26)$$

The output common Mode Range for fig 4.22 is given by:

$$\boldsymbol{OCMR} = V_{OV7}\ To\ VDD - \ V_{SG8} + |V_{TH}| \quad (4.27)$$

The Small signal gain is given by :

$$A_V = A_{V(OTA)} * A_{V(CS)}$$

$$A_V = g_{M1,2}(r_{02}||r_{04}) * g_{m8}(r_{08}||r_{07}) \quad (4.28)$$

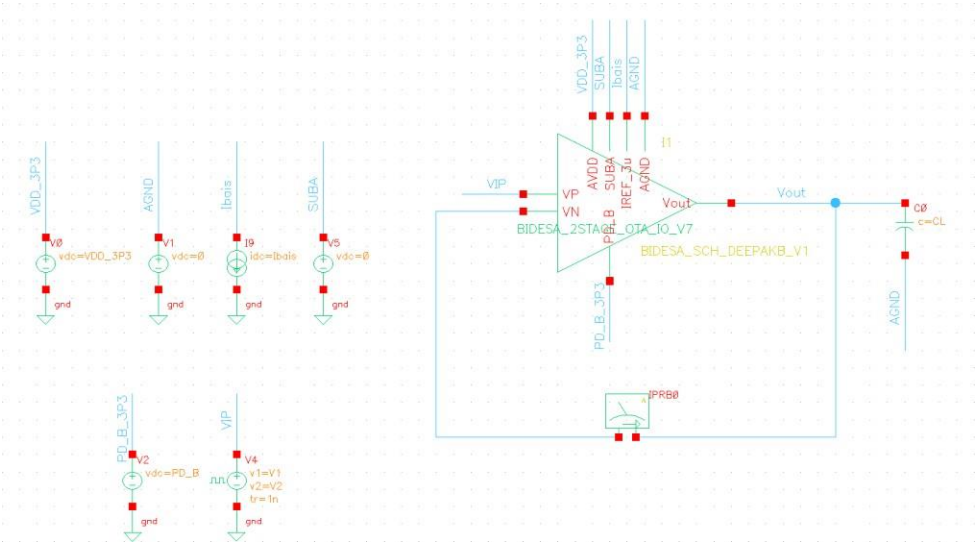

Fig 4.24 – Verification Testbench Setup for the BIDESA_VREF_BUFF

Gain-Bandwidth Product (GBW) is a key parameter of an amplifier, representing the product of the amplifier's open-loop gain and its -3 dB bandwidth. It is a constant value for a given amplifier and is defined as:

$$GBW = A_{OL} * f_{3dB} \quad (4.29)$$

Unity Gain frequency (Single Pole System) for fig 4.22 is

$$GBW = \frac{g_{m1,2}}{C_C} \quad (4.30)$$

Chapter – 5

CMOS Image Sensors

A CMOS image sensor integrates three key components on a single chip: a photosensitive pixel array for image capture, row/column access circuitry for pixel addressing, and dedicated readout electronics for signal processing and output.

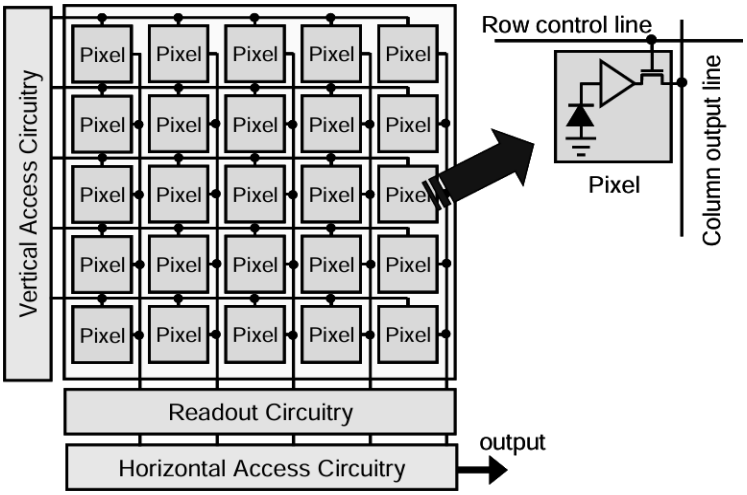

Fig 5.1 - CMOS Image Sensor Architecture

The core imaging component in a CMOS sensor is a grid of light-sensitive pixels, each containing a photodiode and active transistor circuitry. The system employs address decoders to selectively activate individual pixels for data extraction. For signal acquisition, a dedicated readout architecture incorporates switching elements and sampling circuits along each column. Noise reduction is achieved through specialized methods such as correlated double sampling (CDS). The readout process operates row-by-row: pixel charges are first transferred to column-parallel storage elements, then sequentially processed through shared amplification and multiplexing stages before final output.

Types of Pixels –

- Charge-Coupled Device (CCD)
- Passive Pixel Sensor (PPS)
- Active Pixel Sensor (APS – 3T,4T)
- Digital Pixels Sensors (DPS)

A CCD is like a digital film - it captures images by turning light into electric signals at each tiny pixel. Brighter spots create stronger signals. While CCDs used to be in all digital cameras, most new devices now use CMOS sensors because they work better with modern electronics and save battery life."

5.1 Passive Pixel Sensors (PPS)

A Passive Pixel Sensor (PPS) uses a simple structure where each pixel contains just a light-sensitive photodetector and one transistor to read out the signal. The pixel operation is divided into two stages: light-to-charge conversion, where incoming light is converted into an electrical charge, and charge-to-voltage conversion, which is performed externally.

Key Advantages of CMOS Sensors Over CCDs:

1. Higher Integration Capability
2. Reduced System Complexity
3. Improved Power Efficiency
4. Enhanced Readout Performance
5. Increased Flexibility
6. Wide dynamic range imaging
7. On-chip biometric processing
8. Real-time computational photography

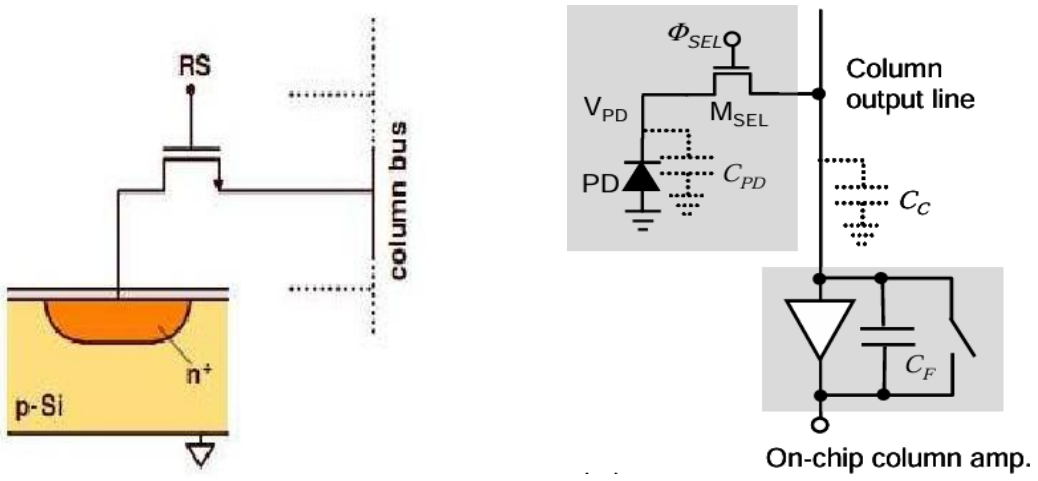

Fig 5.2 Structural and schematic of passive pixel Sensor

5.2 Active Pixel Sensors (APS) (3T & 4T)

An Active Pixel Sensor (APS) is characterized by an active element within each pixel that amplifies the signal. In a common 3T-APS configuration, this includes a photodiode (PD), a source follower transistor (M_{SF}) for signal amplification, and a select transistor (M_{SEL}) for readout. The amplified signal is transferred to the output line, enhancing image quality compared to Passive Pixel Sensors (PPS). In APS, the accumulated signal charge is converted to a voltage at the transistor gate, with voltage gain typically below one.

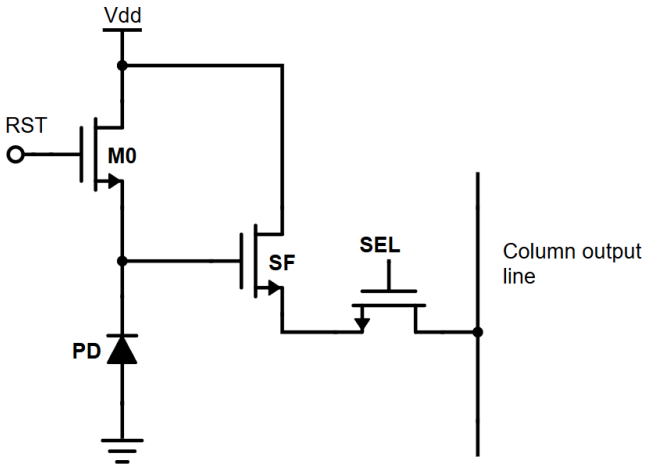

Fig 5.3 – 3 Transistor pixel

The photodiode reset voltage (V_D) in an Active Pixel Sensor (APS) depends on the reset method used :

- Soft Reset: The reset gate is set to VDD, and V_D =VDD−V_{TH} Where V_{TH} is the threshold voltage of the reset transistor, accounting for the body effect.
- Hard Reset: The reset gate voltage exceeds VDD+V_{TH} resulting in $V_D = VDD$

When a photodiode accumulates signal charge Q_{sig} during integration and undergoes soft reset operation (while neglecting access transistor voltage effects), the stabilized output voltage can be expressed as:

$$V_0 = (VDD - V_{TH}) - q\frac{Q_{sig}}{C_D} - V_{GSF} \qquad (5.1)$$

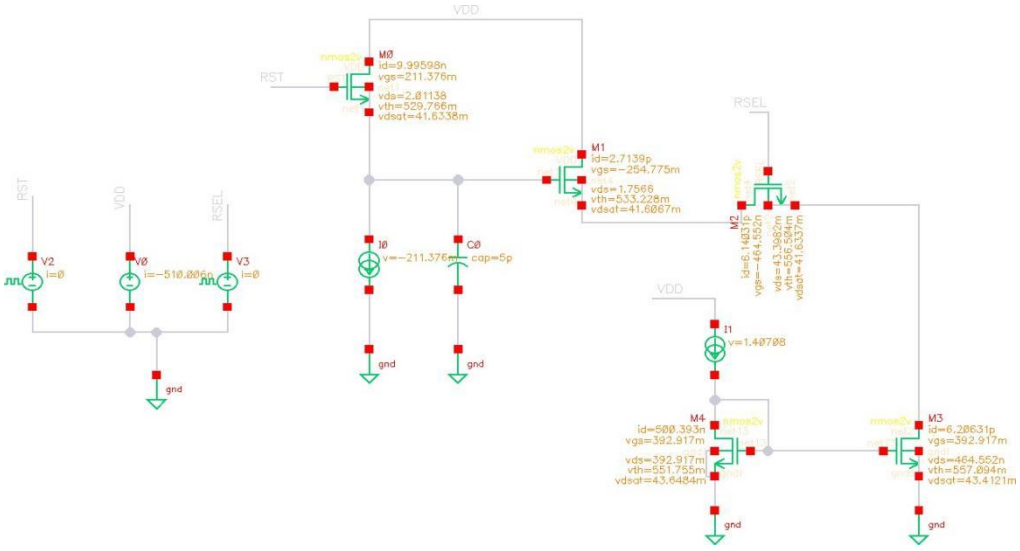

Fig 5.3 – Schematic for the Anlalysis of 3T pixel

For the analysis in Virtuoso, a photodiode was not available; therefore, we used a low-value constant current source, which emulates the current generated by a photodiode, in parallel with a capacitor. This setup replicates the behaviour of a photodiode operating in reverse bias. Initially, the photodiode node is reset using an NMOS-based switch, which is then turned off, allowing the node to hold the reset potential. Upon light illumination, the source follower amplifier tracks the resulting voltage drop (less than the gate-source voltage V_{GS}). Finally, the select switch is activated, transferring this data to the column line for further processing, where the output is taken from the drain of the column line transistor**.**

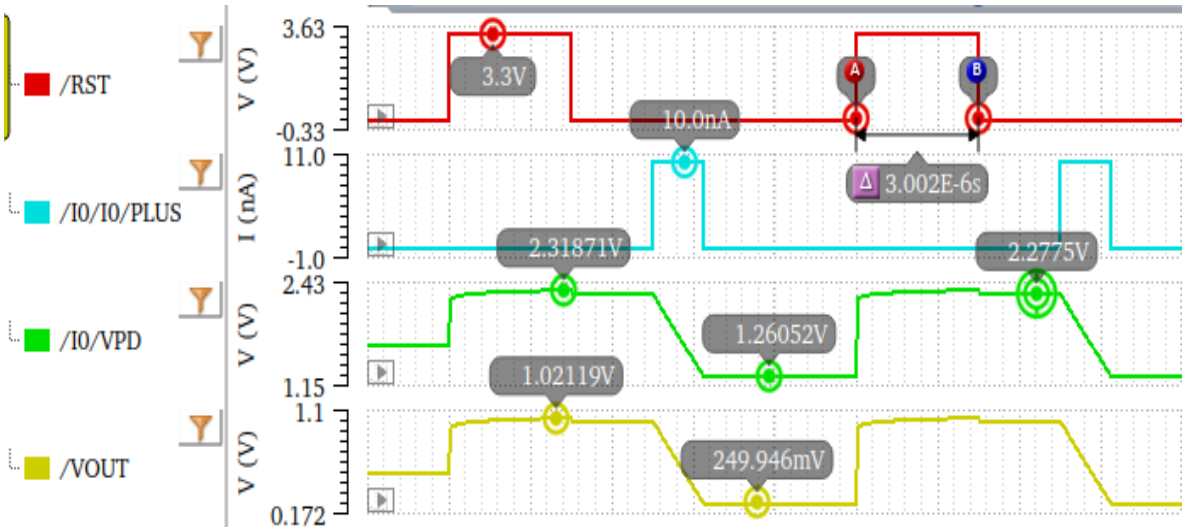

Fig 5.4 – Analyzed Waveform of 3T Pixel

5.2.1 4 – Transistor Active Pixel (4T)

Although Active Pixel Sensors (3TPS) Optimize the signal power relative to the noise floor compared to Passive Pixel Sensors (PPS), they still face challenges, such as difficulty in suppressing k_BT/C noise. In the standard 3T-APS design, the photodiode (PD) serves both as the photodetection and photoconversion region, limiting PD design flexibility. To overcome this, the 4T-APS was developed, Employing distinct zones for photon absorption and electron-hole pair generation Photo-generated charges accumulate in the PD and The generated charges are subsequently shifted to a floating diffusion node for readout (F_D) region, where they are converted to voltage. This configuration uses four transistors per pixel, earning it the name 4T-APS.

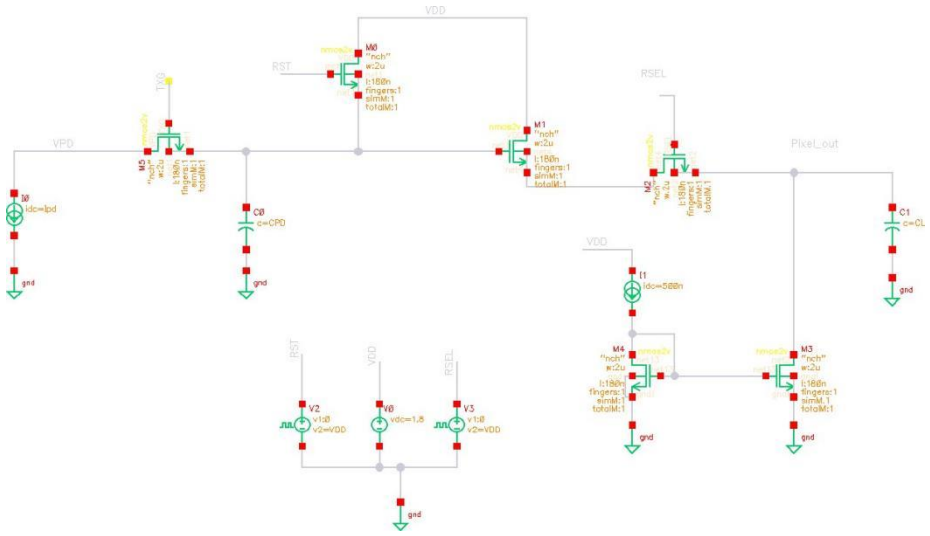

Fig 5.5 4 Transistors Active Pixel

In 4T-APS, the signal charge first accumulates in the photodiode (PD), which is initially fully depleted. Before transferring this charge, the floating diffusion (FD) is reset using the reset transistor ,the reference reset level is captured prior to signal readout to enable correlated double sampling noise reduction. Afterward, the transfer gate is activated to move the accumulated charge from the PD to the FD, followed by readout through the select transistor (MSEL). This CDS process effectively eliminates k_BT/C noise, a feat unattainable in 3T-APS. For optimal performance, the PD must fully deplete during readout, which is achieved using a pinned photodiode (PPD) and a well-designed potential profile for complete

charge transfer.

Fig 5.6 – 4T pixels transient Behavior for Nodes

While the 4T active pixel sensor offers superior noise performance, it introduces several design challenges:

- Reduced Optical Efficiency – The extra transistor required for charge transfer decreases the pixel's light-sensitive area, resulting in a lower fill factor compared to traditional 3T designs.
- Signal Retention Artifacts – Incomplete charge transfer from the photodiode to the floating diffusion node can lead to residual image lag, causing ghosting effects in successive frames.

Process Sensitivity

Optimal performance demands tight manufacturing tolerances for:

- Pinned photodiode doping profiles
- Transfer gate voltage characteristics
- Floating diffusion capacitance matching
- Reset transistor threshold uniformity.

Chapter 6

Low Power Dual Slope ADC

6.1 Weak Inversion Region

In a practical MOSFET, the drain current is not zero even when the gate-to-source voltage (V_{GS}) is below the threshold voltage (V_T). This small but non-negligible current is known as subthreshold current, occurring in the subthreshold region where $V_{GS}<V_{TH}$. Despite being below the threshold, a positive drain current can still flow, primarily due to diffusion. This weak inversion region is characterized by a gradual increase in drain current as V_{GS} approaches V_T, and the current is governed by an exponential relationship between the drain current and V_{GS}:

$$I_D = \frac{W}{L} I_{DO} e^{qV_{GS}/\eta kT} \qquad (6.1)$$

where η and I_{DO} can be extracted from experimental data. In the subthreshold regime $V_{GS} - V_{TH} < 0$, MOSFET drain current exhibits exponential voltage dependence like bipolar transistors. This occurs because current flow is dominated by diffusion mechanisms rather than drift. The resulting ultra-low current levels make this operating region ideal for low-power circuit design, where minimizing static power consumption is critical.

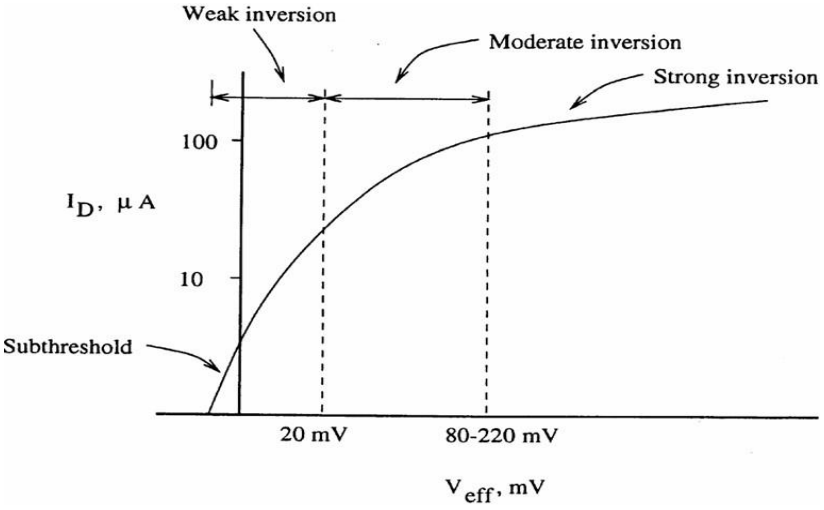

Fig 6.1 – Drain current as a function of overdrive voltage

6.2 Integrating Type ADC

For measuring stable voltages or slowly fluctuating signals, integrating-type ADCs provide superior conversion fidelity, offering high accuracy with a simple, low-cost design. Known for their excellent linearity, noise rejection, and minimal offset and gain errors, these converters achieve high resolution but have slow conversion rates, typically requiring 2^N clock cycles for standard single or dual-slope designs. Due to their slow speed, they are unsuitable for signal processing or audio applications but excel in high-precision tasks such as driving electronic displays (LCD/LED) and instrumentation devices.

6.2.1 Dual Slope Architecture

The dual-slope conversion technique represents a class of integrating analog-to-digital converters that of ADC that converts an unknown input voltage (V_{IN})into a digital value using an integrator. The conversion process begins with the input voltage applied to the integrator for a fixed duration known as the run-up period (t_R). During this period, the integrator output ramps up proportionally to the input voltage.

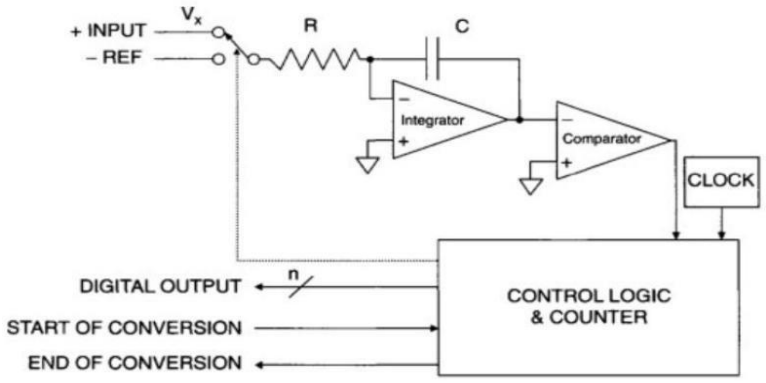

Fig 6.2 Structure Dual Slope ADC

So, the output of the integrator will be given as:

$$V_{OUT} = -V_C = \int_0^{t_1} \frac{V_{IN}}{RC}\, dt \tag{6.2}$$

$$V_{OUT} = -\frac{V_{IN} T_1}{RC} \tag{6.3}$$

Since the V_{IN} is constant in nature the capacitor will follow up linear behaviour for the constant current so output will be opposite of that of capacitor voltage and will get a ramp

and that will be compared by the comparator. Following the run-up, a known reference voltage (REF) of opposite polarity is applied, causing the integrator output to ramp down until it reaches zero. The time taken for this ramp-down (run-down period) is measured and used to determine the input voltage. Unlike single-slope ADCs, the dual-slope approach compares the integrator output to ground, allowing it to integrate both the unknown The measured input signal and precision reference potential.

$$V_{Out} = V_{intital} + \int_{T1}^{T2} -(\frac{V_{ref}}{RC})dt \quad (6.4)$$

$$V_{out} = -\frac{V_{IN}T_1}{RC} + \frac{V_{ref}T_2}{RC} \quad (6.5)$$

At last, the V_{out} will become zero so :

$$T_2 = (V_{IN}\,T_1)/V_{ref} \quad (6.6)$$

From here we can observe the there is no dependency upon the Resistor and capacitor Initially, a negative input is applied to the integrator, producing a positive ramp at the output until a predefined count limit is reached (2^Nclock cycles). The incoming signal subsequently switched to the reference voltage, which causes a downward ramp, and the counter measures the clock cycles The ratio T2/T1 provides the digital representation of the input voltage.

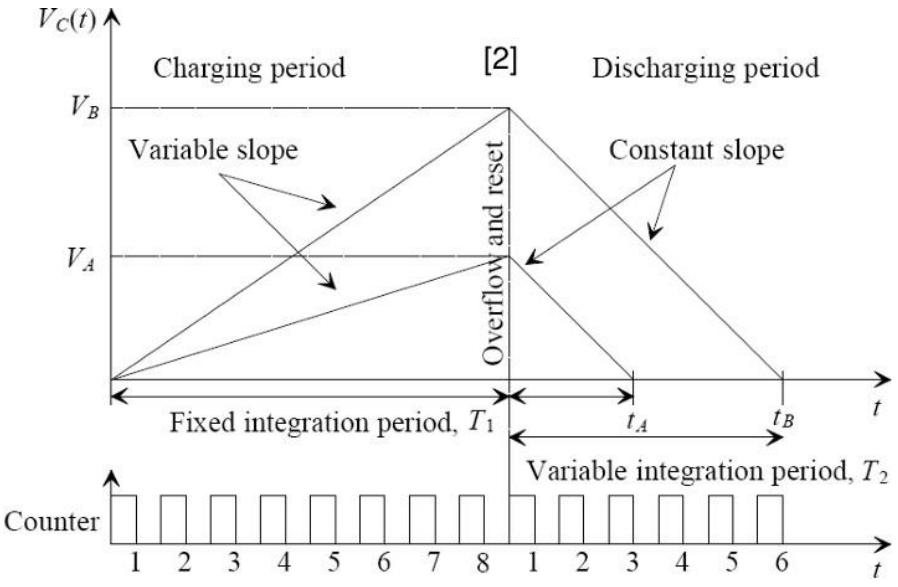

Fig 6.3 Transient Behaviour of Capacitor

A key advantage of the dual-slope method is its inherent noise and error cancellation. Errors related to the integrator's resistor and capacitor (RC) values, as well as clock jitter, are minimized because the same components are used for both the run-up and run-down periods. However, this accuracy comes at the cost of conversion speed, as the process requires up to 2^{N+1} clock cycles.

6.3 Critical Parameters in Amplifier Stage Design

In the architectural planning of MOS analog signal paths, factors such as channel width, quiescent drain current, and frequency response are critical. The -3 dB cutoff frequency and mid-frequency gain characteristics primarily guide the design, while parameters like channel length and power consumption are adjusted based on gain and frequency requirements. Operating in the weak inversion region (below strong inversion) can be beneficial for low-frequency circuits like op-amps. This approach offers several advantages:

1. Maximum small-signal gain occurs in the transitional region (0.1V < V_OV < 0.2V) before full strong inversion.
2. Lower power consumption due to reduced current.
3. Minimized distortion, with more consistent gain over a wider current range and reduced even harmonic distortion.

These benefits are especially useful in low-frequency applications where BW is not an issue.

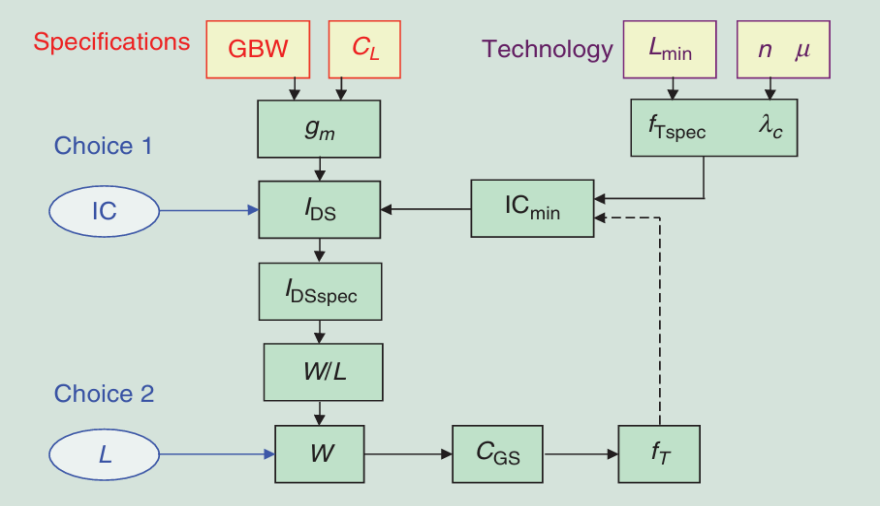

Fig 6.4 – The design procedure for an amplifier [2]

This work introduces an innovative bulk-driven input stage design that achieves superior performance metrics, including extended output voltage range and increased DC gain, relative to traditional bulk-driven differential pair configurations. These improvements are achieved without relying on partial positive feedback, avoiding the common drawbacks typically associated with such methods.

6.4 Circuit Description of Bulk Driven 2 stage OTA

The operational amplifier utilizes an input stage with a PMOS configuration, optimized using n-well technology. This approach is chosen because it allows for separate well formation for PMOS transistors, making it suitable for implementing body biasing a technique critical for low-power design. By using body biasing, the threshold voltage can be dynamically controlled, enhancing the performance and power efficiency of the amplifier.

In this design, transistors M_{1A} and M_{1B} constitute a differential transistor pair employing gate biasing through diode-configured devices (M_{2A} & M_{2B}) and stabilized using a current sink (M_{4A}& M_{4B}). The bulk terminals of M_{1A} and M_{1B} are cross-coupled with those of M_{2B} and M_{2B}, respectively, allowing for differential input application. Specifically, the differential input signal is applied between the bulk terminals of M_{1A} and M_{1B} on one side and M_{1B} and M_{2A} on the other, effectively modulating the threshold voltages of these transistors.

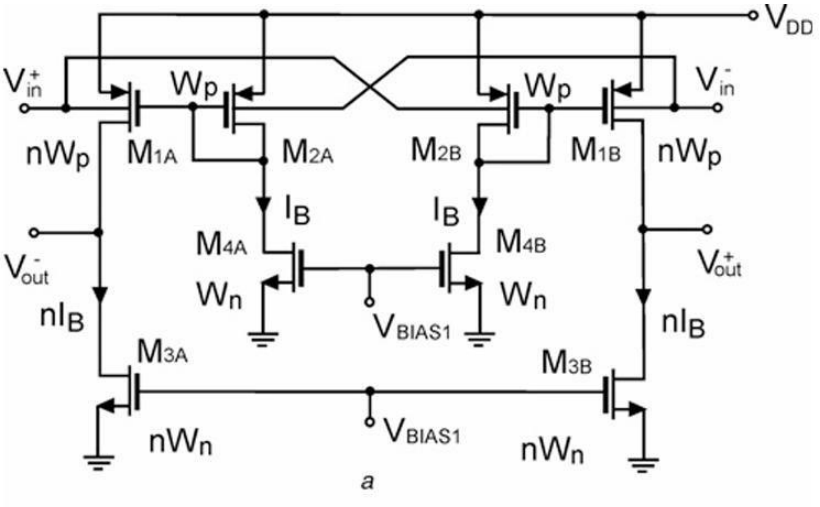

Fig 6.5 – Bulk driven Differential Amplifier [4]

In this configuration, the gate and drain voltages of $M_{2A}$and M_{2B} are directed to the gates of M_{1A} and M_{1B}, providing dual control of the input transistors through both their bulk and gate terminals. This dual control mechanism enhances the transconductance of the input stage by dynamically adjusting the drain currents of M_{1A} and M_{1B}.

Assuming the inputs are shorted and controlled by a common-mode signal (V_{CM}), and the circuit maintains perfect symmetry, the source-gate (V_G) and bulk-source (V_{BS}) voltages of all PMOS transistors are identical. Under these conditions and ignoring the effect of the limited output resistances of MOSFETs can influence the drain currents of M_{1A} and M_{1B} remain constant directly linked to the magnitude of the drain currents M_{4A} and M_{4B}.

Based on these assumptions, the amplifier demonstrates immunity to input common-mode fluctuations, effectively functioning as a true differential amplifier. A significant advantage of the proposed design over a standard bulk-driven differential pair is its enhanced output voltage range. The highest and lowest voltage levels at each output of the circuit in Fig. 4a can be determined by the following conditions.

$$V_{max,6.5} = V_{DD} - V_{DSsat} \quad (6.7)$$

$$V_{min,6.5} = V_{DSsat} \quad (6.8)$$

The circuit is designed to operate with a minimal supply voltage of $V_{DD_{\min}} = 2V_{DSmin}$ V_{DSat} represents the voltage at which the MOS transistor enters saturation is referred to as its saturation voltage. Despite the low supply voltage, the design maintains excellent common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and rail-to-rail input common-mode range (ICMR). Additionally, the circuit functions in class AB mode, which enhances its slew rate (SR) performance.

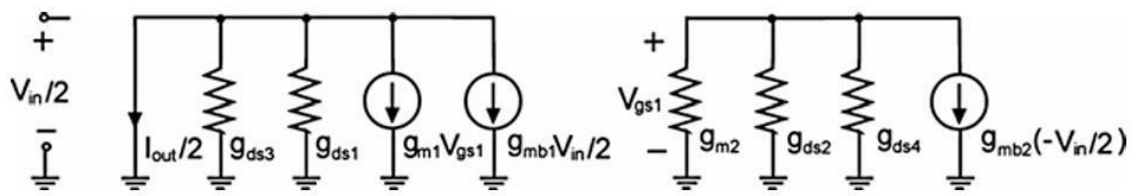

Fig 6.6 – Small-signal equivalent half-circuit of the amplifier of Fig. 6.5

For small-signal analysis, a symmetrical configuration is assumed for the circuit, with the analysis based on using the half-circuit analysis technique, we derive a small-signal model representing one side of the differential pair under linear operating conditions. During this analysis, the amplifier outputs are considered Connected to ground for AC signals, allowing for an accurate derivation of the small signal transconductance of the input stage.

The output current $I_{out}/2$ can be expressed as

$$I_{OUT}/2 = -(g_{mb1}V_{IN}/2 + g_{m1}V_{GS1}) \qquad (6.9)$$

$$V_{GS1} = -\frac{g_{mb2}}{g_{m2}+g_{ds2}+g_{ds4}}(-V_{in}/2) \qquad (6.10)$$

Substituting (6.10) into (6.9), after elementary derivations we obtain

$$\frac{I_{out}}{2} = -g_{mb1}\left(1 + \frac{g_{m1}}{g_{mb1}}\frac{g_{mb2}}{g_{m2}+g_{ds2}+g_{ds4}}\right)\frac{v_{in}}{2} \qquad (6.11)$$

Thus, the DC transfer conductance characterizing the amplifier's current-to-voltage conversion $gm_{eff\ 6.5}$ is given by

$$g_{meff,1a} = g_{mb1}\left(1 + \frac{g_{m1}}{g_{mb1}}.\frac{g_{mb2}}{g_{m2}+g_{ds2}+g_{ds4}}\right) \qquad (6.12)$$

For the same V_{bs} voltages for transistors $M_{1A,B}$ and $M_{2A,B}$ at the operating point, we have $g_{m1}/g_{mb1} = g_{m2}/g_{mb2}$. Assuming further that $g_{m2} \gg (g_{ds2} + g_{ds4})$, the circuit transconductance can be approximated as

where the symbols have their usual meaning.

$$g_{meff\ 1,a} \cong 2g_{mb1} \qquad (6.13)$$

The feed-forward path exhibits negligible impact on the OTA's DC open-loop gain, which is given by

$$A_{v0} \cong \frac{2g_{mb1}}{g_{ds1}+g_{ds3}} \qquad (6.14)$$

while the GBW product is

$$GBW = \frac{2g_{mb1}}{c_c} \qquad (6.15)$$

6.4.1 Implementation and Analysis of the Circuit

The proposed amplifier, shown in Fig. 6.7,is a two-stage Miller operational transconductance amplifier (OTA) with an additional feedforward path in the second stage to counter the right-half-plane (RHP) zero caused by the compensation capacitor C_C. The second gain stage is formed by transistor M_1, which is loaded by transistor M_{21}, and C_C is used for frequency compensation. In conventional Miller OTAs, C_C introduces a parasitic RHP zero that degrades the phase margin (PM) and limits the gain-bandwidth product (GBW). To address this, a series resistor is added in the feedback path of the compensation capacitor, effectively shifting the RHP zero and improving both stability and bandwidth. This design ensures that all MOS transistors operate in the subthreshold region, optimizing power efficiency.

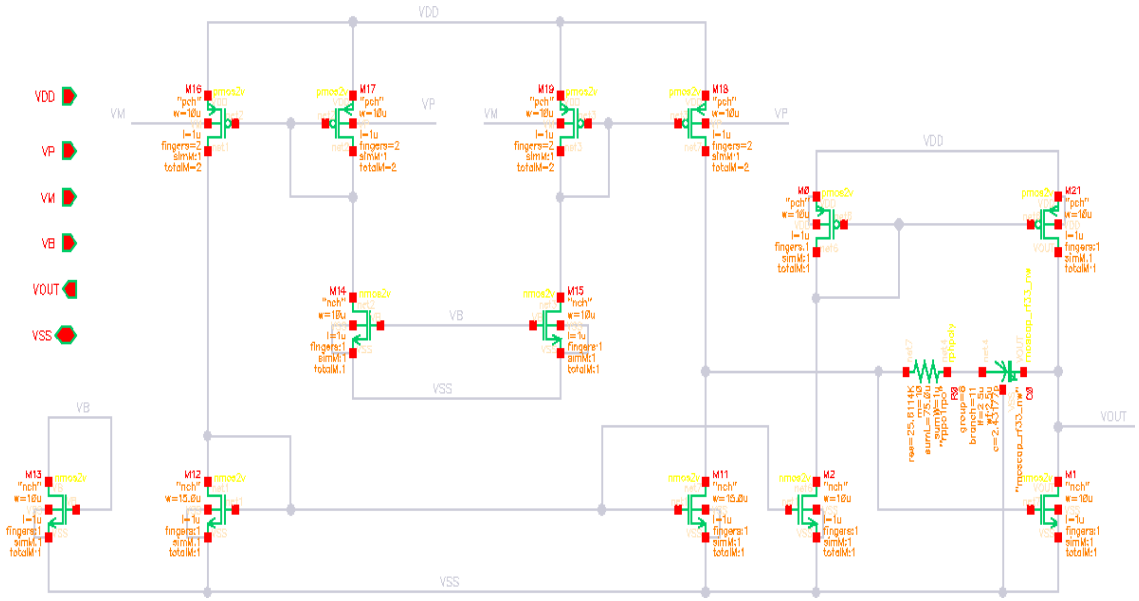

Fig 6.7 – Proposed Structure for the Two Stage Bulk Driven Op-amp [3]

The proposed OTA has been designed in a 0.18-µm CMOS process from Taiwan Semiconductor Manufacturing Company (TSMC). The circuit was designed for VDD = 0.5 V, Given operation in the deep subthreshold regime (V_GS << V_TH) with these parameters: GBW = 45 kHz, CL = 1 pF, PM = 60◦, and the dynamic range (DR) = 60 dB. The biasing current I_B was calculated based on the assumed input noise and DR [3]. It was

also assumed $M_1 = M_2$ for optimal noise performance and $M_9 = M_4$. This entails $I_{D1} = I_{D2} = I_B$. For the calculated value of IB (50 nA), the input transconductance (2gmb1) was 480nS using the assumed value of GBW, the compensation capacitance CC was 3 pF, and the value of the resistor is 300K.

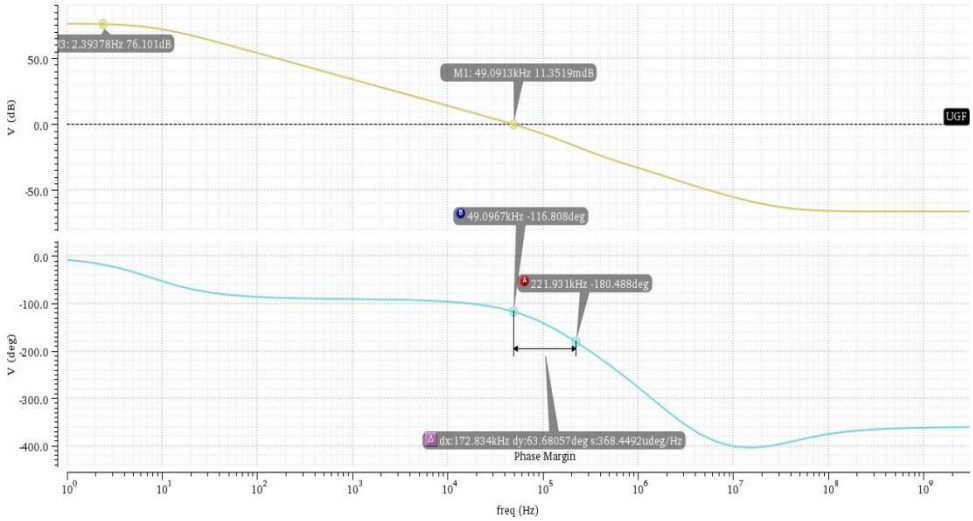

Fig 6.8 – Differential Mode Gain and Phase plot of the Two Stage Op-amp

In case of ideal symmetry of the input stage, the dc CMRR may be expressed as

$$CMRR = \frac{g_{m2}+(g_{ds2}+g_{ds4})/2}{(g_{ds2}+g_{ds4})/2} \cong \frac{g_{m2}}{(g_{ds2}+g_{ds4})/2} \qquad (6.16)$$

The dc PSRR for the two circuits was derived for inputs shorted to ground for ac signals. The dc PSRR for the circuit of Fig. 4a can be approximated as .

$$PSRR \cong \frac{2g_{mb1}}{g_{ds1}+n[g_{ds4}(1+(\frac{g_{mb2}}{g_{m2}}))+g_{ds2}((\frac{g_{mb2}}{g_{m2}}))]} \qquad (6.17)$$

The sizing parameters (W/L ratios) were systematically adjusted post-biasing, with channel lengths deliberately oversized to boost intrinsic gain . Larger L in the input stage also entails the larger transistor channel areas, which allows decreasing the input-referred offset and flicker noise.

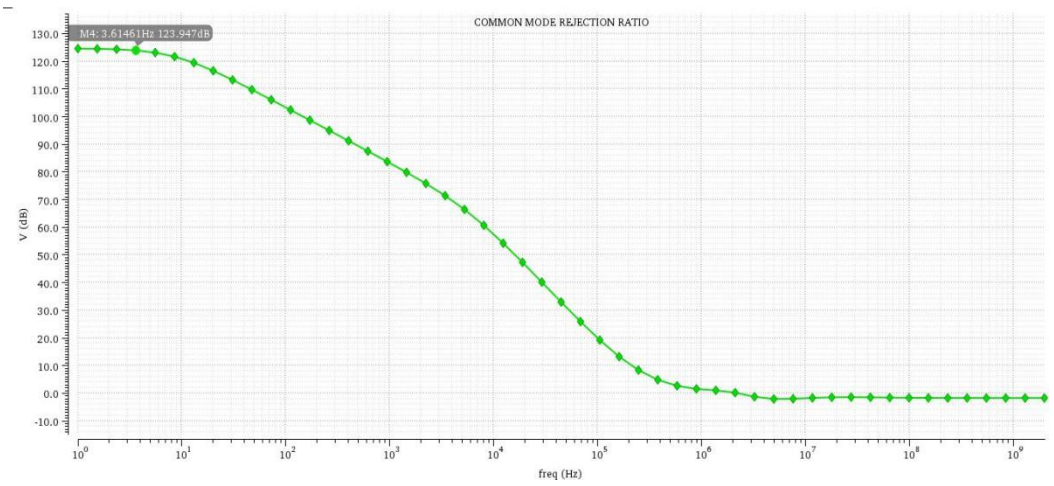

Fig 6.9 – Common Mode Rejection Ratio (CMRR) Plot for the Op-Amp

The channel widths were adjusted to achieve $|V_{GS}| \approx V_{DD}/2$ at the operating point. With the Simulation We got to Know that the bare minimum bias current and vdd under all PVT variations we calculated the minimum Power as 176.6 nW with all Device Working Properly according to our design Aspects.

Table 4 Result Showing the Op-amp MOSFET and Circuit Parameter

Test	Output	Min	Max	Mean	Median	Std Dev	Spec	Pass/Fail
OP_AMP_ANALYSIS	Power_consumption	162.8n	191.3n	177.1n	177.5n	8.401n		
OP_AMP_ANALYSIS	OS("/I0/M19" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OP_AMP_GAIN_VALUE	73.24	77.97	75.87	76.04	1.081		
OP_AMP_ANALYSIS	OS("/I0/M0" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OS("/I0/M2" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OS("/I0/M1" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OS("/I0/M21" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OS("/I0/M11" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OS("/I0/M12" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OS("/I0/M13" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OS("/I0/M14" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OS("/I0/M15" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OS("/I0/M16" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OS("/I0/M17" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	OS("/I0/M18" "region")	3	3	3	3	0		
OP_AMP_ANALYSIS	PM	-128.1	-109.5	-119.1	-119.7	5.598		

Table 5 Aspect ratios and Miller Compensated values

Aspects Ratios	Values
W/L ($\boldsymbol{M_1}$ & $\boldsymbol{M_2}$)	10µm / 1µm
W/L ($\boldsymbol{M_{11}}$ & $\boldsymbol{M_{12}}$)	15µm / 1µm
W/L ($\boldsymbol{M_{13}}$ & $\boldsymbol{M_{14}}$)	10µm / 1µm
W/L ($\boldsymbol{M_{15}}$ & $\boldsymbol{M_{21}}$ & $\boldsymbol{M_{01}}$)	10µm / 1µm
W/L ($\boldsymbol{M_{16}}$ & $\boldsymbol{M_{17}}$)	40µm / 1µm
W/L ($\boldsymbol{M_{18}}$ & $\boldsymbol{M_{19}}$)	40µm / 1µm
$\boldsymbol{R_c}$	200K
$\boldsymbol{C_c}$	3pF

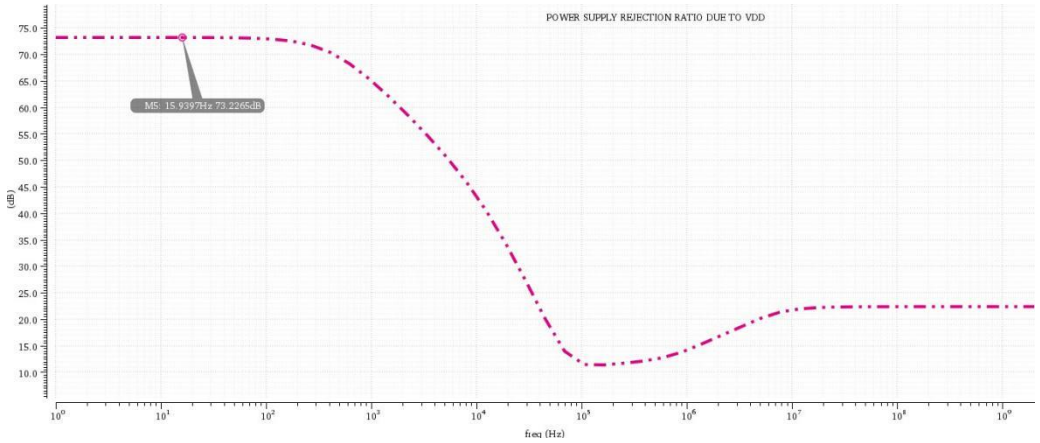

Fig 6.10 – Power Supply Rejection Ratio (PSRR) due to VDD plot for the Op-amp

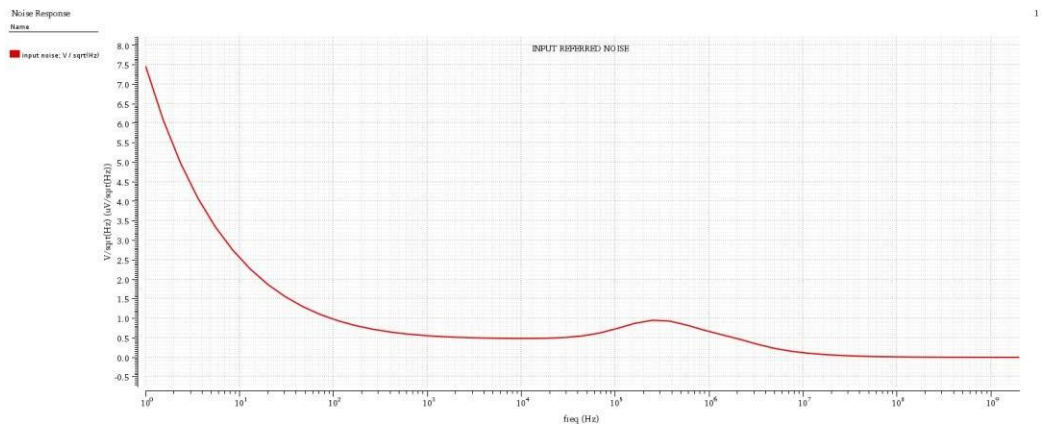

Fig 6.11 – Input refereed noise of the op-amp

Stability analysis in Cadence Virtuoso with I-Probe is used to measure loop gain and phase margin accurately without altering the circuit's operating point. It simplifies setup and provides direct visualization of gain and phase, making it easy to detect stability issues.

Table – 6 Stability Summary with Loop Probe

Stability Parameter	Values
Phase Margin	71.431° @ 50.2 kHz
Gain Margin	13.613 dB @ 271.4 kHz

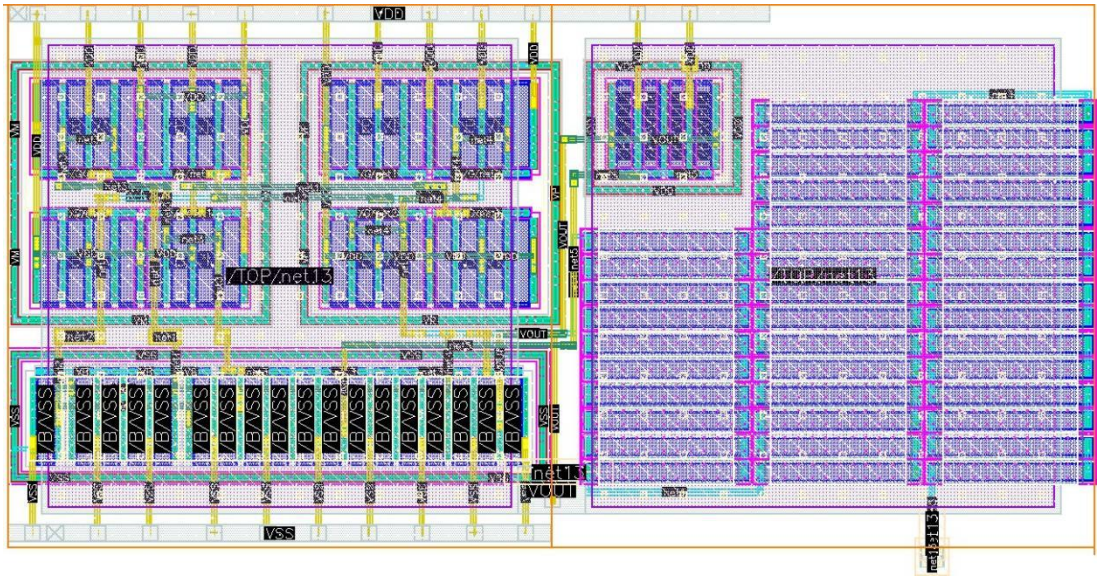

Fig 6.12 Layout for the BD 2 stage OTA

For the layout of the bulk-driven two-stage OTA, a common centroid matching technique was employed for the differential pair, ensuring precise matching and minimizing mismatch errors. Even-numbered metal layers were assigned for vertical connections, while odd-numbered metal layers were used for horizontal connections. To prevent latch-up issues, guard rings were implemented for body connections, providing effective isolation. The series resistor used in the design was carefully laid out, and the layout successfully passed design rule check (DRC), layout versus schematic (LVS), and parasitic extraction.

DRC (Design Rule Check) is a verification process in layout design that ensures the layout adheres to foundry-specific geometric and connectivity rules. It checks for violations like minimum width, spacing, overlap, and enclosure of various layers (metal, poly, diffusion, etc.). Passing DRC ensures the layout is manufacturable and avoids issues like short circuits, open circuits, or lithography problems.

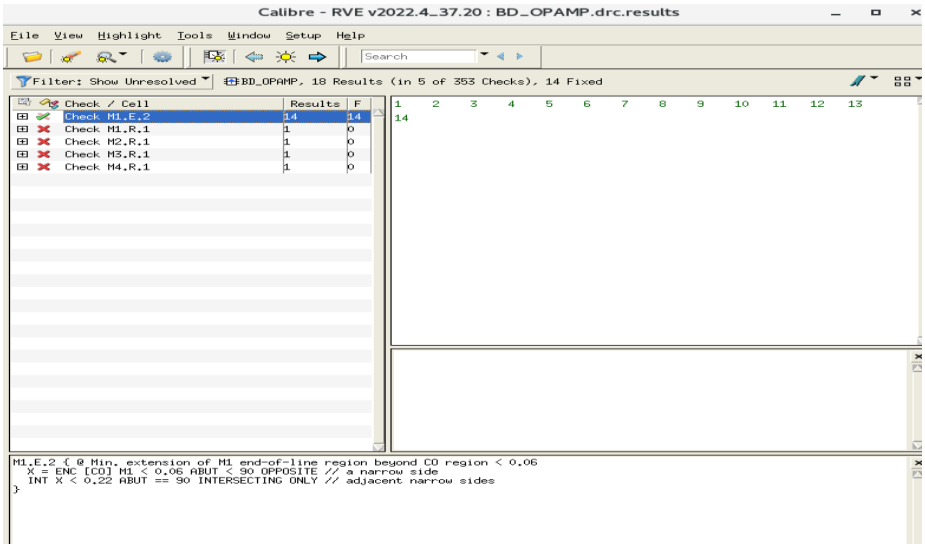

Fig 6.13 DRC Check Validation for BD-OTA

LVS (Layout Versus Schematic) - is a verification process that ensures the layout design matches the intended schematic at the netlist level. It checks for correct connectivity, device types, sizes, and parameters between the layout and the schematic. Passing LVS confirms that the layout accurately implements the circuit design without any unintended changes or mismatches.

Fig 6.14 LVS Check validation for BD-OTA

Table 7 Performance Summary and Comparison of operational Amplifier

Parameters	5 Transistor – OTA	Telescopic Cascode OTA	Bulk Driven OTA
Tech Node	TSMC 180nm	TSMC 180nm	TSMC 180nm
VDD	1.8 V	1.8 V	0.5 V
Reference Current	10µA	25µA	50nA
ICMR Range	783mV	468mV	-
DC Gain (dB)	40.98dB	69.2dB	35.99 dB
GBW (Hz)	10.06 MHz	6.3 MHz	244.7kHz
Load capacitance	1p	3p	1p
Phase Margin	88.85°	89.19°	77.28°
CMRR (dB)	77.39 dB	104.37 dB	85.10 dB
PSRR (dB)	82.36 dB	155.78 dB	73.22 dB
Slew Rate (V / µs)	7.62	0.446	18.39 (V / ms)

6.5 Applications of the Low Power Op-amp

6.5.1 Practical Active Integrator

An integrator generates an output voltage representing the accumulated input signal over time. Passive integrators use only R/C components, while active integrators (e.g., op-amp-based) provide precision and stability. This analysis covers active implementation

Due to the op-amp's negligible input current, the current I through resistor R_1 must equal the current through C_f . From input side we can write

$$I = \frac{V_{in}-V_A}{R_1} = \frac{V_{in}}{R_1} \qquad (6.18)$$

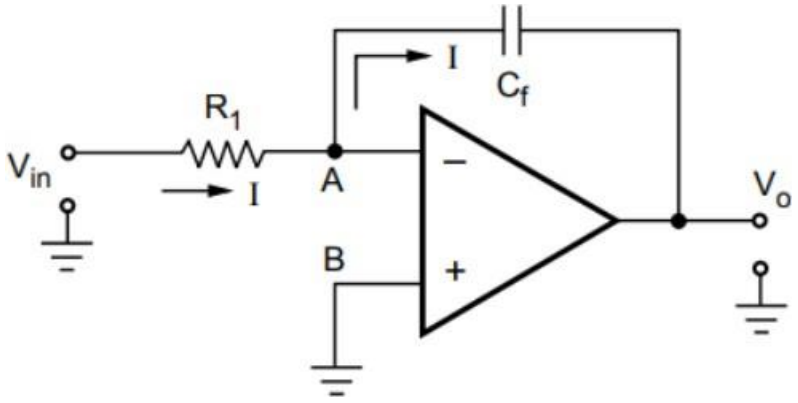

Fig 6.15 Op-amp Ideal Integrator Circuit

From output side we can write,

$$I_C = -C_f \frac{dV_0}{dt} \qquad (6.19)$$

Integrating both sides,

$$\int_0^t \frac{V_{in}}{R_1}\, dt = -C_f \int \frac{dV_0}{dt} dt \qquad \textbf{(6.20)}$$

$$V_0 = -\frac{1}{R_1 C_f}\int_0^t V_{in}\,dt + V_0(0) \qquad (6.21)$$

The equation (6.21) shows that the output is $-1/R_1C_f$ times the integral of input and R_1C_f is called time constant of the integrators.

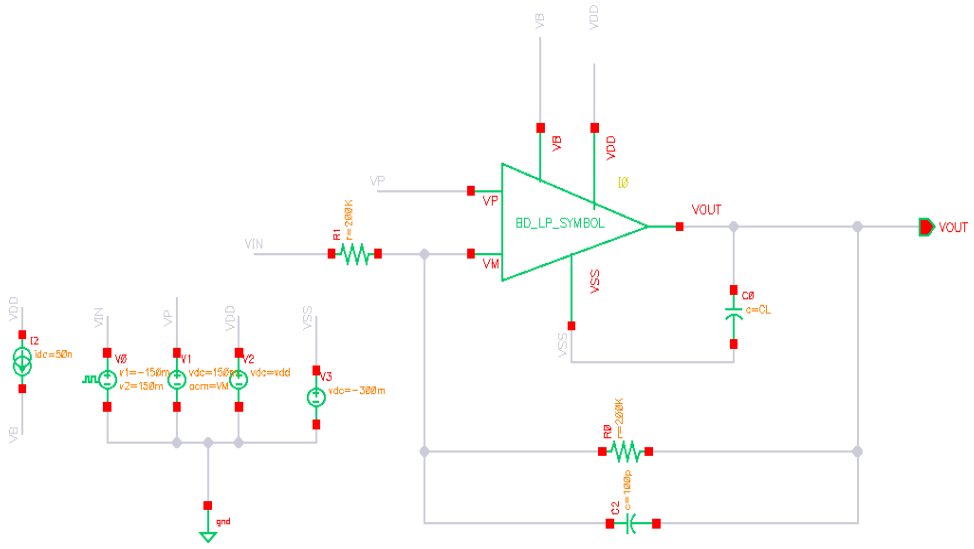

Fig 6.16 Op-amp Testbench for The Practical Integrator

For the Proper integration time constant $R_fC_f >> T_p$ of the input Signal.

Here C_F = 100pF , R_F = 200 K So R_fC_f = 20µS and T_p = 400nS

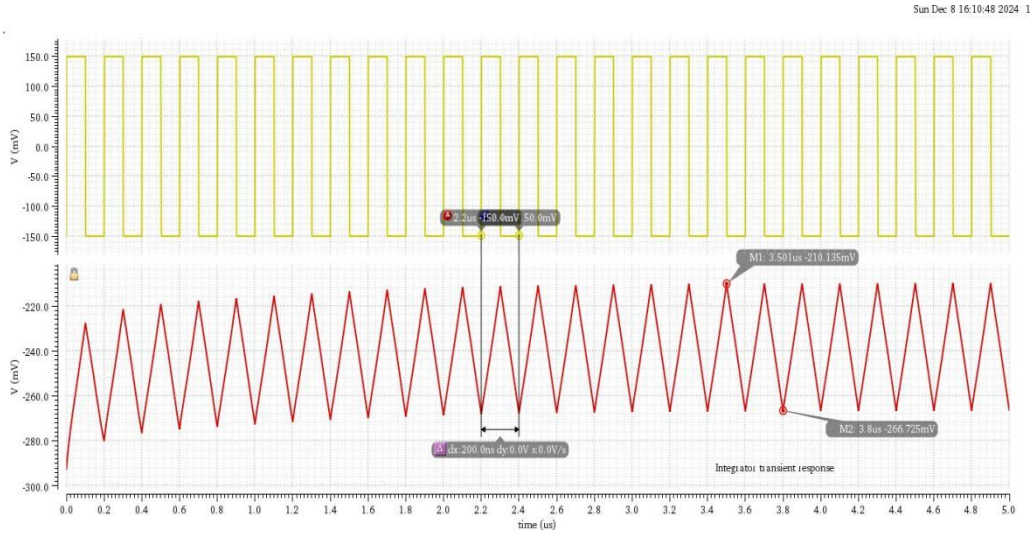

Fig 6.17 Transient Response for the Pulse Input to the bulk driven op-amp integrator

For an op-amp integrator with a pulse input, the output is a linearly varying voltage whose slope is proportional to the amplitude of the input pulse and its duration. A positive pulse produces a decreasing (negative slope) output, while a negative pulse generates an increasing (positive slope) output. After the pulse ends, the output holds the last value reached until another input is applied.

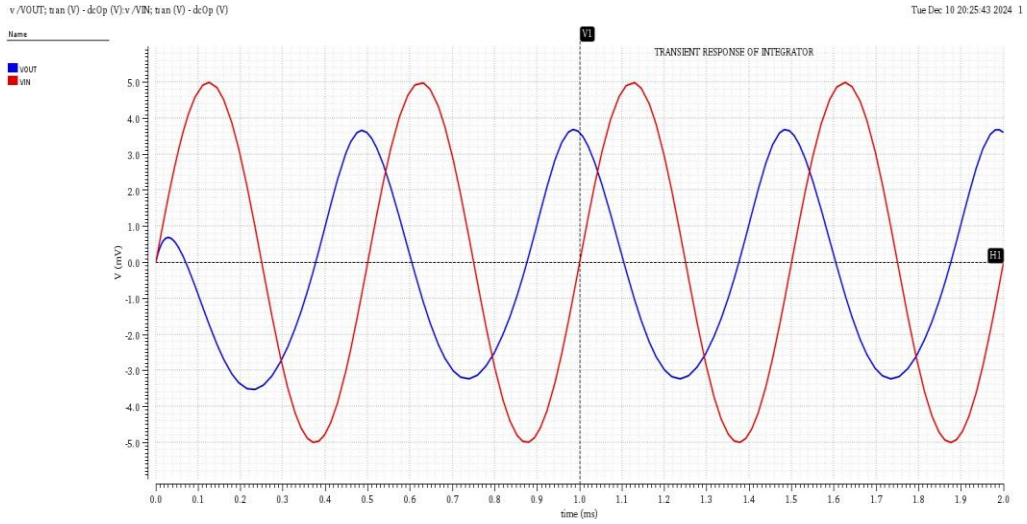

Fig 6.18 – Transient Response for the Sinusoidal input

6.5.2 Low power Comparator

A comparator is an electronic circuit that compares two input signals and generates an output indicating which input is higher or lower. In an op-amp-based comparator operating in open-loop configuration, the output saturates to one of the supply rails depending on which input is higher. However, one common issue with comparators is offset voltage, which can cause unwanted variations in the output, leading to inaccurate comparisons**.**

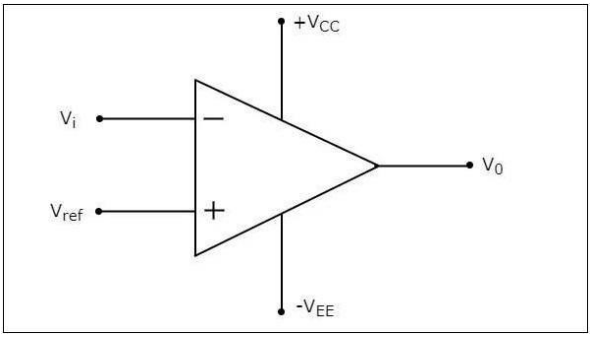

Fig 6.19 Inverting Comparator

An inverting comparator is a circuit that compares an input voltage (v_i) with a reference voltage (V_{ref}). It produces one of two output values, $+V_{sat}$ or $-v_{sat}$, depending on the comparison:

- If the input voltage is greater than the reference voltage, the output is -V_{sat}.
- If the input voltage is less than the reference voltage, the output is +V_{sat}.

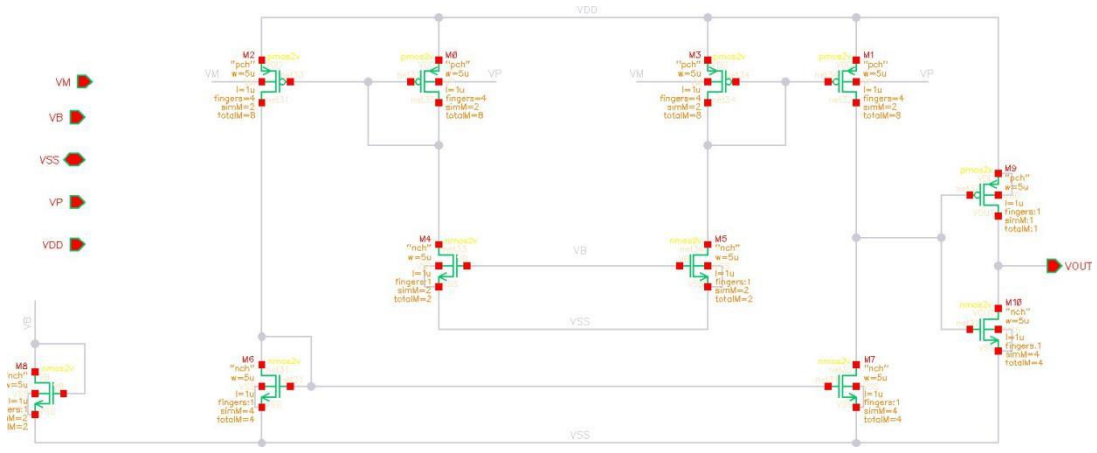

Fig 6.20 – Schematic of Low Power Comparator

For the low-power comparator design, a bulk-driven (BD) OTA differential stage is used at the input, providing enhanced sensitivity at low supply voltages. The output of this stage is cascaded with an inverter, which ensures a rail-to-rail output range (0 to VDD). The voltage transfer characteristic (VTC) of the inverter is carefully matched within the output range of the BD OTA, guaranteeing accurate and fast switching while maintaining efficient low-power operation.

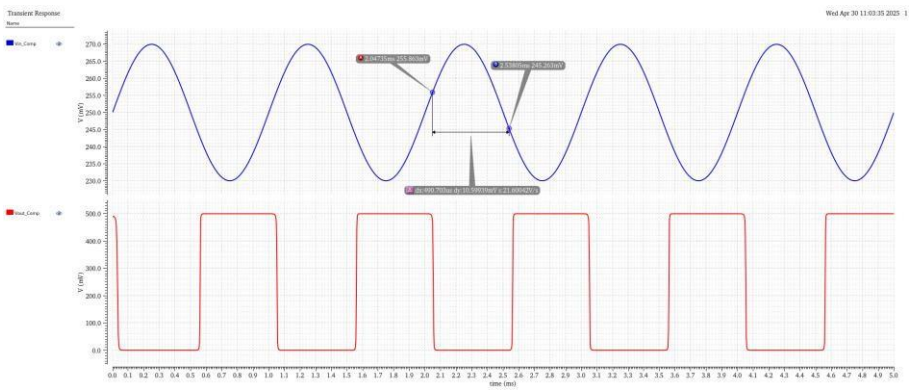

Fig 6.21 – Transient response of the comparator

6.6 Merging Comparator and Integrator

In a dual-slope ADC, the integrator ramps up or down in response to the input voltage Vin over a fixed period. The comparator monitors the integrator's output and switches when it reaches a threshold, marking the end of the integration phase.

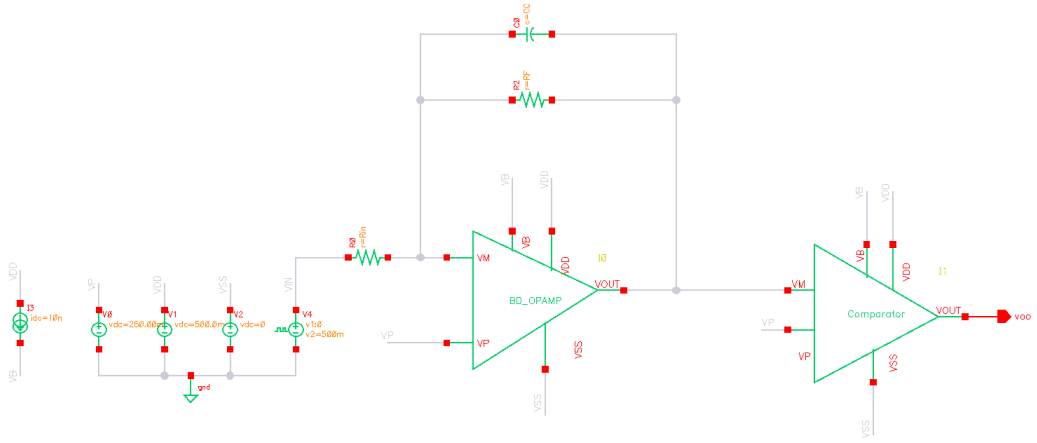

Fig 6.22 – Integrator And Comparator Testbench

During the de-integration phase, the reference voltage is applied, and the output returns to zero. The time taken for this reset is proportional to Vin, enabling the ADC to convert the input signal into a digital value with high accuracy.

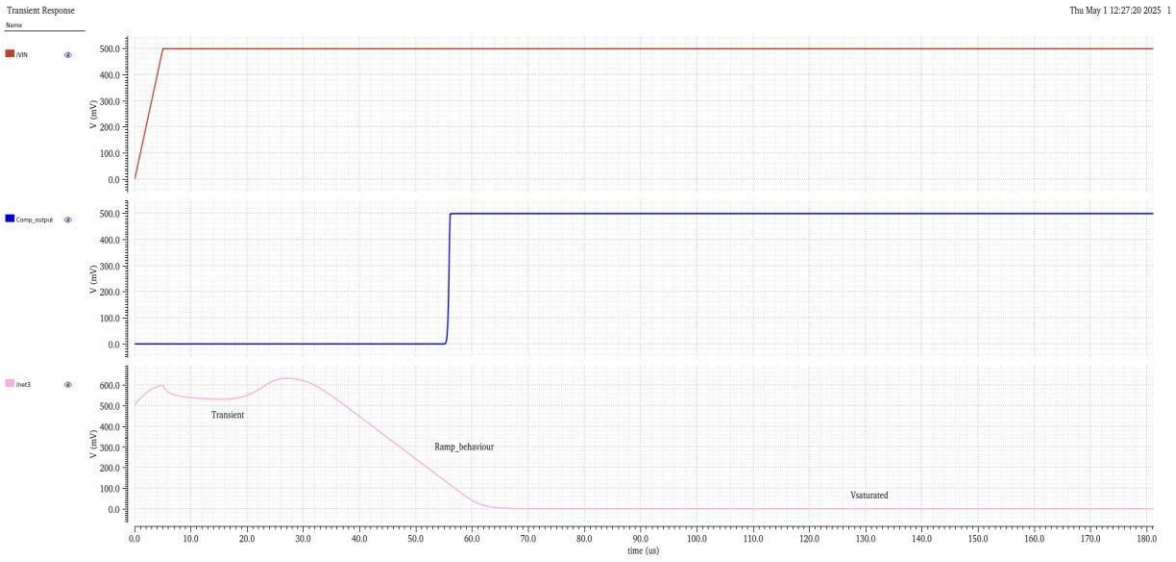

Fig 6.23 Step response for the together integrator and comparator

When a step input is initially applied, the capacitor in the integrator is shorted, causing a constant current to flow due to the virtual short condition. As a result, the integrator's output will ramp linearly. Once the ramp voltage exceeds 250 mV, the comparator outputs a logic low. When the ramp voltage falls below 250 mV, the comparator will output a logic high, rising directly to VDD.

Chapter – 7

Conclusion and Future Scope

In this report, we introduced an innovative ultra-low-voltage bulk-driven operational amplifier with a new differential input stage. Our proposed design stands out from traditional bulk-driven amplifiers by providing superior low-voltage capability and enhanced DC voltage gain. It offers a practical and efficient solution for ultra-low-voltage OTAs, showcasing remarkable power efficiency and improved CMRR in a compact and reliable structure. The design incorporates essential components such as the common source single-stage amplifier, differential amplifier, and current mirror, which contribute to its performance and efficiency.

The experimental results validate the performance of our design, showing that it can operate effectively even at the lowest VDD/VTH ratios reported in literature. Our comparison of various design strategies highlights that the proposed OTA1 design is the best option for applications requiring ultra-low-voltage operation, while alternative structures with voltage gain boosting techniques can be considered when higher voltage gain is needed. Overall, our design provides a competitive and reliable solution for ultra-low-voltage OTA applications.

The future of low-power bulk-driven techniques in VLSI design looks promising. They are ideal for portable devices, IoT applications, biomedical gadgets, energy harvesting systems, and environmental monitoring. As technology advances, these efficient circuits will help create more energy-saving and powerful devices.

Bibliography

1. Design of Analog CMOS Integrated Circuits / Behad Razavi, Professor of Electrical Engineering, University of California, Los Angeles. – Second edition
2. Analog Design Essentials by Willy M. C. Sansen, Catholic University, Leuven, Belgium.
3. Ohta, J. (2020). *Smart CMOS Image Sensors and Applications* (2nd ed.). CRC Press.
4. Liu, Y., & Theuwissen, A. J. P. (2012). The design of a high dynamic range cmos image sensor in 110nm technology. *Delft University of Technology*, 1-34.
5. Nagyt, L., Arbet, D., Kovac, M., Potocny, M., Sovcik, M., & Stopjakova, V. (2021, April). Ekv mos transistor model for ultra-low-voltage bulk-driven ic design. In *2021 24th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS)* (pp. 6-10). IEEE.
6. Kulej, T., & Khateb, F. (2019). A compact 0.3-V class AB bulk-driven OTA. *IEEE Transactions on Very Large-Scale Integration (VLSI) Systems*, *28*(1), 224-232.
7. Kulej, T. (2013). 0.5-V bulk-driven CMOS operational amplifier. *IET Circuits, Devices & Systems*, *7*(6), 352-360.
8. Shan, H., Rausch, S., Jou, A., Conrad, N. J., & Mohammadi, S. (2017, January). A low power programmable dual-slope ADC for single-chip RFID sensor nodes. In *2017 IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)* (pp. 118-120). IEEE.